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Effect of gate oxide thickness on polycrystalline silicon thin-film transistors

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ABSTRACT

This work presents the study of the effect of gate oxide thickness on the performance of lightly doped polycrystalline silicon thin-film transistors with large grains. It is observed that scaling down of the oxide thickness is an efficient way to reduce the threshold voltage and hence to improve the poly-Si TFT characteristics. A reasonably good fitting between the analytical results and the experimental data support the validity of this model.

KEYWORDS

Polysilicon;
Gate oxide;
Threshold voltage;
TFTs.

INTRODUCTION

The major attractions of applying polycrystalline silicon thin-film transistors(poly-Si TFTs) in active-matrix liquid crystal displays(AMLCDs) lie in the greatly improved mobility in poly-Si film and the capability to integrate panel array and peripheral driving circuit on the same substrate[1-3]. For these applications, scaled-down poly-Si TFTs with high performance and high reliability are required[4]. Polysilicon film generally consists of grains separated by grain boundaries. In this film, few trap states exist in the grains while many trap states exist at the oxide-silicon interface and grain boundaries. Though the presence of grain boundary traps has a profound effect on the performance of poly-Si TFT but their contribution can be reduced by decreasing the number of grain boundaries. Using modern MILC technique or excimer laser annealed methods, it is possible to create devices where only a single or small number of discrete grain boundaries exist in the channel of the poly-Si TFT[5-7]. Different other process techniques have been investigated to improve the device performance of the transistors with reduced number of grain boundaries and recently a new device structure called the triple gate poly-Si TFT (TG-TFT) has been proposed[8], considering a single grain boundary in the channel of poly-Si TFT.

In this model it is assumed that the oxide-silicon interface traps are evenly distributed throughout the interface region and channel of poly-Si TFT contains single grain boundary. Based on this idea, the aim of this paper is therefore to propose an analytical model that presents the effect of gate oxide thickness on threshold voltage and hence on the characteristics of poly-Si TFTs. The obtained results indicate an effective way to improve the polysilicon thin film transistor characteristics.

THEORY

The device structure used to develop the model is shown in figure 1. The drain current in the linear region of operation of a large grain polysilicon TFT can be adequately described by the relation[9]

$$I_D = (Z/D)\mu_{eff} C_{ox} (V_G - V_T)V_D \quad (1)$$

where Z/D is the channel width to channel length ratio, μ_{eff} is the effective carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_D is the drain voltage and V_T is the threshold voltage.

In order to calculate the threshold voltage the band bending at the interface in the semiconductor of the device is determined by using Poisson's equation:

$$d^2\Phi/dx^2 = -\rho/\varepsilon_s \ldots \quad (2)$$

where Φ is the electrostatic potential, ε_s is the dielectric constant of polysilicon material and ρ is the charge density which can be written in terms of density of states $N_T(cm^{-3} eV^{-1})$ in the polysilicon film, as

$$\rho = -q^2 N_T \Phi \ldots \quad (3)$$

In terms of electric field, eq (2) can be written as;

$$EdE/d\Phi = q^2 N_T \Phi/\varepsilon_s \ldots \quad (4)$$

Now integrating from the bulk toward the surface yields

$$\int_{Bulk}^{Surface} EdE = (q^2 N_T/\varepsilon_s) \int_{Bulk}^{Surface} \Phi d\Phi \ldots \quad (5)$$

As E and Φ are zero in the bulk therefore we get;

$$E_s = q\Phi_s (N_T/\varepsilon_s)^{1/2} \ldots \quad (6)$$

where E_s is the surface electric field and Φ_s is the surface potential.

Now under the strong inversion condition at threshold[10] we have

$$\Phi_{s(inv.)} = 2\Phi_F = (2kT/q) \ln (N_A/n_i) \quad (7)$$

where $\Phi_{s(inv.)}$ is the surface potential under inversion condition, k is Boltzmann's constant, N_A is acceptor doping density and n_i is the intrinsic carrier density of the semiconductor.

The oxide (insulator) electric field, E_{ox}, is related to E_s by the relationship

$$E_{ox} = (\varepsilon_s/\varepsilon_{ox})E_s \ldots \quad (8)$$

where ε_{ox} is the dielectric constant for the oxide. At threshold, the gate oxide electric field is

$$E_{ox\,(inv.)} = (\varepsilon_s/\varepsilon_{ox})[(2kT) \ln (N_A/n_i) (N_T/\varepsilon_s)^{1/2}] \quad (9)$$

Now the voltage across the insulator, V_{ox}, is simply equal to $t_{ox}E_{ox}$ where t_{ox} is the oxide thickness. The threshold voltage is therefore given by

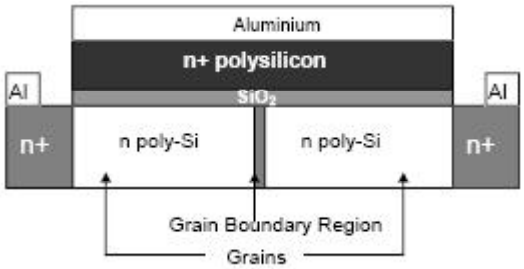

Figure 1: Structure of the poly-Si TFT with oxide-silicon interface

$$V_T = \Phi_{s(inv.)} + V_{ox\,(inv.)} \quad (10)$$

$$V_T = (2kT/q) \ln (N_A/n_i) [1 + q(t_{ox}/\varepsilon_{ox})(\varepsilon_s N_T)^{1/2}] \quad (11)$$

In polysilicon TFT, the effective carrier mobility is affected by the potential barrier height ψ_B due to grain boundaries and number of grains n in the channel, through the relationship[11]:

$$\mu_{eff} = \frac{\mu_G}{1 + [n-1]\mu_G D_{GB} / n\mu_{GB} D_G] \exp(q\Psi B / kT)} \quad (12)$$

where D_G is average grain size, D_{GB} is average grain boundary width, μ_G is the bulk grain mobility and μ_{GB} is the mobility in the grain boundary. In this model n =2.

The height ψ_B of the potential barrier which exists at the grain boundary in an idealized poly-Si film is given by[12]

$$\psi_B = q\, n_t^2 / 8N\varepsilon_s \ldots \quad (13)$$

where n_t is the grain boundary trap-state density.

For an n-channel TFT, once inversion is reached, the total charged carrier concentration is approximately equal to the gate-induced carrier (electron) concentration. Hence the carrier concentration, N in the strong inversion channel, in terms of gate voltage is given as[13]

$$N = C_{ox}(V_G - V_T)/q\, t_{si} \quad (14)$$

Hence eq (13) becomes

$$\Psi_B = \frac{q^2 n_t^2 t_{si}}{8\varepsilon_S C_{ox} (V_G - V_T)} \quad (15)$$

where t_{si} is the polysilicon film thickness.

RESULTS AND DISCUSSION

The typical values of the model parameters used in the calculations are given in TABLE 1. Figure 2 (a) and (b) shows the calculated values of threshold voltage as a function of trap density and doping concentration for various values of gate oxide thickness. It is seen that

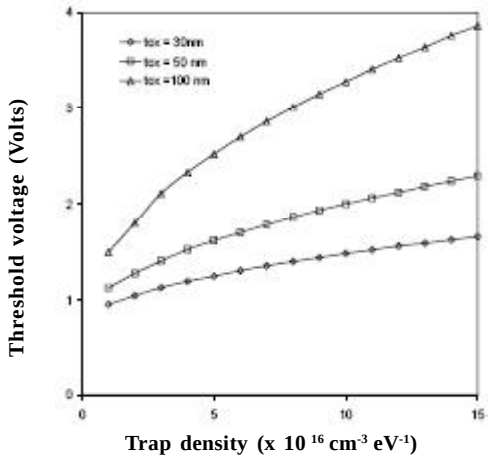

Figure 2(a): Computed variation of threshold voltage as a function of trap density for different values gate-oxide thickness at room temperature

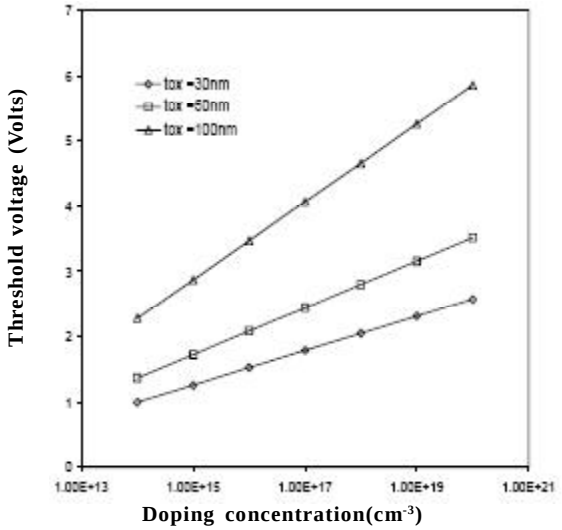

Figure 2(b): Computed variation of threshold voltage as a function of doping concentration for different values gate-oxide thickness at room temperature

TABLE 1: Parameters used in the study

Parameters	Symbols	Values
Channel length	D	10μm
Channel width	Z	10μm
Grain boundary width	D_{GB}	2 nm
Drain voltage	V_D	0.1 volt
Acceptor density	N_A	10^{16} cm^{-3}
Polysilicon inversion layer thickness	t_{si}	4nm
Bulk grain mobility	μ_G	203cm^2/V-sec
Grain boundary mobility	μ_{GB}	0.3cm^2/V-sec

with the decrease in gate oxide thickness, threshold voltage decreases as defects present in the oxide layer decreases. It is further noted that for a particular value of

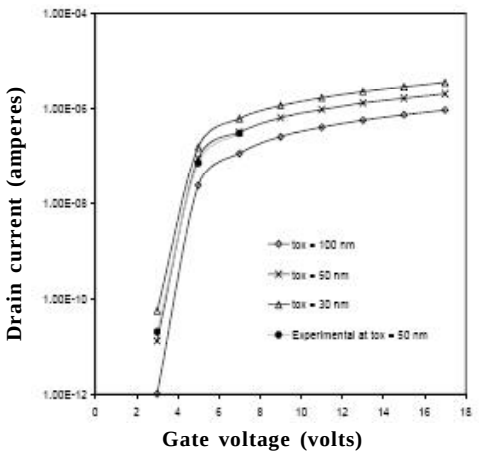

Figure 3: Computed variation of drain current with gate voltage at various oxide thickness values at room temperature. Dark circle shows the experimental results given by Li and Lin[18]

gate oxide thickness, threshold voltage increases with increase in doping concentration.

Furthermore, it is also noticed that the difference in the threshold voltage for three different values of gate oxide thickness is less in lower doping concentration side as compared to high doping concentration side. This may be attributed due to the fact that at high doping concentration, the grains become partially depleted and also the concentration of trap states is large and these trap centers act as voltage source resulting in larger scattering of the carriers thereby increasing the potential barrier across the channel of the device.

Figure 3 illustrates the computed variation of drain current with gate voltage for different values of oxide thickness, t_{ox}. It is observed that for all values of t_{ox}, drain current increases rapidly with the increase in gate voltage which is due to the gate-induced barrier lowering effects. It is also observed that as gate oxide thickness decreases, drain current increases which may be due to the lowering of trap states at the oxide-silicon interface of the poly-Si TFT. Moreover for a sufficiently thin gate oxide, the motion of carriers is also influenced by the mirror image of the zig-zag wall dipole in the heavily doped gate. When the gate conductor plane is near the channel, the dipole is screened and the potential barrier for the in-plane motion of carriers becomes lower. This effect results in an increase in the channel mobility which in turn increases the drain current. Therefore scaling down of the gate oxide thickness is an effi-

cient way to improve the characteristics of a poly-Si TFT. But the disadvantage of scaling down the gate oxide is the enhancement of the leakage current at large drain bias voltages. However, researchers reported that this undesirable effect can be effectively suppressed by using lightly-doped drain[14,15], field-induced-drain[16] or off-set gated[17] structures. The results so obtained are compared with the available experimental data of Li and Lin[18] for t_{ox} = 50nm. Excellent fitting between the calculated results and the experimental data support the validity of this model.

CONCLUSION

In this paper, a model for calculating the threshold voltage of polysilicon TFTs incorporating the effect of gate oxide thickness is proposed. In this model it is assumed that the oxide-silicon interface traps are uniformly distributed and the channel of the device contains only a single grain boundary. Calculations reveal that for a particular value of gate oxide thickness, threshold voltage decreases with decrease in trap density and doping concentration and as gate oxide thickness decreases, threshold voltage decreases for given trap density and doping concentration. In order to improve the poly-Si- TFT characteristics, it is desirable to decrease the gate oxide thickness below 30nm. The analytical results are compared with the experimental data and are shown to be in satisfactory agreement.

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