Analytical model of threshold voltage and sub-threshold slope of SOI and SON MOSFET: A comparative study

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ABSTRACT

A threshold voltage model based on three-interface compact capacitive model is developed for horizontal SOI/SON MOSFET. Different short channel effects like drain induced barrier lowering, 2-D charge sharing and fringing field effects are considered. Analytical simulation is done to understand the threshold voltage performance of silicon on insulator (SOI) and silicon on nothing (SON) MOSFET, under different structural and operational parameter variations. The performance of the two devices are studied and compared in terms of threshold voltage roll-off and subthreshold slope. Performance of SON MOSFET is found to be significantly different from equivalent SOI device. SON MOSFET demonstrates lower threshold voltage roll-off and subthreshold slope due to reduced short channel effects. Present analysis is found to be useful to figure out the improvement of SON over SOI structures as a next generation short channel MOS structure.
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INTRODUCTION

With the emergence of mobile computing and communication, low power device design and implementation have got a significant role to play in VLSI circuit design. Continuous device performance improvement is possible only through a combination of device scaling, new device structures and material property improvement to its fundamental limits[1]. The down-scaling of MOSFETs has been the most important and effective way for achieving device performance improvement for VLSI/ULSI circuits. Increased demand for ultra low power consumption, high density and high performance devices is continuously pushing the fabrication process to go beyond the sub-micron technologies such as 45nm, 32nm and so on. However, the performance requirement in these advanced technologies couldn't be achieved with conventional bulk CMOS process leading to an alternative, Silicon-on-Insulator (SOI) technology[2]. Short-channel-effects (SCEs), transistor scalability, and circuit performance are improved by using SOI technology, especially ultrathin, fully depleted (FD) MOSFETs[3]. MOSFET fabricated on insulator (SOI) substrate provides an advantage for high speed applications because of the low parasitic capacitance. As CMOS IC technology enters the sub-
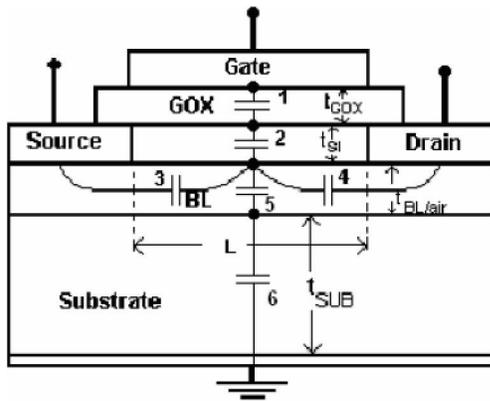
Figure 1 : A SOI/SON-MOSFET layered structure

TABLE 1 : Parameters for simulation

Parameters	Value
N_A	$0.5 \times 10^{14} \text{cm}^{-2}$
N_{SUB}	$4 \times 10^{12} \text{cm}^{-2}$
V_B	0V
V_{DS}	1V
T	300K
t_{GOX}	5nm
t_{BOX}	147nm

50 nm range, the silicon channel and the buried oxide thicknesses must be less than 50 nm and 100 nm, respectively, in order to prevent the short channel effect (SCE)[4]. The development of SOI MOSFET technology has been limited so far by the difficulty in controlling the silicon film thickness, adjusting buried oxide layer thickness, shallow source drain series resistances and the fringing fields[5-7]. A super SOI, having a silicon film thickness of five nanometers and a buried oxide thickness of 20 nm might be capable of suppressing the SCE at the CMOS down-scale limit of 20 nm channel length, however, the requirements for the exceptionally thin silicon and buried oxide films exceed present manufacturing capabilities for SOI wafers[8].

Although different SCEs are highly suppressed in SOI structure, SOI structure is not fully immune to different SCEs. Among different SCEs related device performance degradation, higher threshold voltage roll-off and degraded subthreshold slope are very important issues[9]. To overcome such types of drawbacks in usual SOI structure, different improved SOI structures are suggested in recent times[10]. Silicon-on-Nothing (SON), an innovative SOI structure suggested and developed very recently, enables fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) super SOI devices, which are capable of quasitotal suppression of SCEs and excellent electrical performances[11]. In a SON MOSFET, the buried layer of usual SOI MOSFET is replaced with air which causes less SCEs and leakage currents. Among the advantages of fully-depleted (FD) SON architecture comparing to FDSOI, the most significant one is the reduced electrostatic coupling of channel with source/drain and substrate through the buried layer (BL)[12]. Reduced elec-

trostatic coupling through the BL allows in turn to reduce the minimal channel length of transistors or to relax the requirements on Si film thickness[13]. Moreover, since the so-called ''nothing'' (or air) layer embedded below the Si active film has lower dielectric permittivity than oxide, the parasitic capacitances between source/drain and substrate are reduced and therefore higher circuit speed can be expected with SON devices. Thick buried layer can be a drawback of SOI MOSFETs due to large positive charge accumulated in the thick BL, while in the case of SON MOSFET, no charge will accumulate in the air-gap[14].

Although SOI and SON structures have basic resemblance, accurate modeling of different short channel effects is essential as their influences are different in those structures. Adopting similar theoretical approach developed previously for SOI MOSFET threshold voltage modeling[15], threshold voltage model of horizontal SON MOSFET have been previously established[11]. In this work, a generalized three-interface compact capacitive model of horizontal SOI/SON MOSFET has been developed. Different SCEs like fringing field, substrate coupling and junction-induced 2D-effects are incorporated in the present model. A new approach has been adopted for fringing field capacitance calculation. Analytical expressions of threshold voltage and subthreshold slope including the fringing capacitance effect are developed from the compact capacitive analysis. The performance of the two devices are studied and compared in terms of threshold voltage roll-off and subthreshold slope.

Analytical modeling

In a short channel device, potential profiles in the channel and beneath the channel (in the BL) are two-dimensional in nature. Assuming a parabolic potential profile initiated by perpendicular and lateral field, thresh-
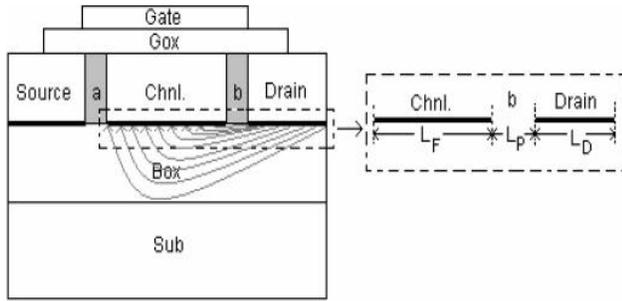
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Figure 3 : Fringing capacitance model of SOI/SON-MOSFET

Figure 2 : Equivalent capacitance model of SOI/SON-MOSFET

old voltage can be calculated by solving 2-D Poisson's equation in the channel[16]. It can also be calculated by solving 1-D Poisson's equation and than incorporating lateral field effect through voltage doping transformation (VDT). This type of analysis is commonly known as compact capacitive model and this model predicts threshold voltage with almost same accuracy as with 2-D Poisson's equation but with less complexity[16].

Equivalent capacitive model

A generalized layered structure of a SOI/SON MOSFET is shown in figuer 1. The structure considered here has poly silicon (n+) gate. Let t_{GOX}, t_{Si}, $t_{BL/air}$ and t_{sub} be the thicknesses of gate oxide, silicon channel layer, buried layer and substrate layer respectively. L is the metallurgical channel length of the device.

A simple compact-capacitance model developed for the description of the threshold voltage V_{th} of the fully depleted SOI/SON-MOSFET is shown in figure 2.

In the figure, $C_{if(1,2,3)}$ are the interface state capacitances for three interfaces, $C_{Si,d}$ is the silicon channel depletion capacitance, C_{GOX} is the gate oxide capacitance C_B is the capacitance due to substrate bias, C_F^D and C_F^S are the fringing field capacitances from drain and source side respectively. V_{FB1} is the flat band voltage at the front interface of the channel due to gate; V_{FB2} is the flat band voltage at the channel back interface due to source/drain; V_{FB3} is the flat band voltage at the back interface of the channel due to substrate.

Short channel effects

For a long channel device, it can be considered that the gate is completely responsible for depleting the channel. In a short channel device, some part of the depletion is accomplished by the influence of drain voltage as well as channel back interface potential; this
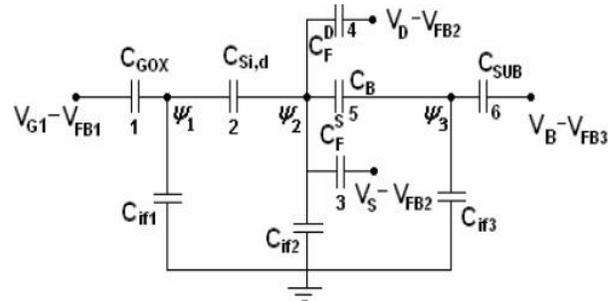
phenomenon is known as two dimensional charge sharing effect[17]. In terms of potential this can be explained on the basis of potential barrier lowering at source-channel junction due to lateral field in the channel initiated by applied drain voltage and this phenomenon is commonly known as drain induced barrier lowering (DIBL). Another component of DIBL is caused by induced potential at channel back interface[17]. Under short channel condition, channel back interface potential is due to combined effect of substrate bias, hole accumulation and fringing field.

DIBL due to lateral field

Voltage doping transformation is a technique, which can be used to take into account the effect of channel lateral field related DIBL into quasi 1D threshold voltage analysis[16]. According to VDT, the effect of lateral field in the channel from drain side is equivalent to a reduction in the effective channel doping. Using VDT for modeling short channel effects, the effective channel doping is given by[11];

$$N_A^* = NA - \frac{2\varepsilon_{Si}V_{DS}^*}{qL_{eff}^2} \qquad (1)$$

Here, ε_{Si} is the dielectric constant of silicon, q is the electronic charge, N_A is the silicon impurity doping concentration, V_{DS}^* is the effective drain to source voltage which is given by;

$$V_{DS}^* = V_{DS} + 2(V_{bi} + \Psi_{S2} - \Psi_{S1}) + \\ 2\sqrt{(V_{bi} + \Psi_{S2} - \Psi_{S1})(V_{DS} + V_{bi} + \Psi_{S2} - \Psi_{S1})} \qquad (2)$$

Here V_{DS} is the drain-to-source voltage, V_{bi} is the built in potential, ψ_1 and ψ_2 are the channel front and back interface potential, respectively. Appling voltage doping transformation, the effective channel depletion capacitance is given as;
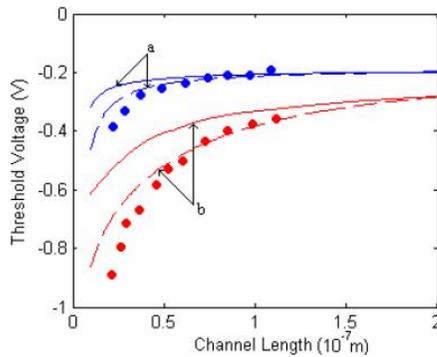
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Figure 4 : Plot of Threshold voltage with channel length for SOI (dashed line) and SON (solid line) MOSFET. Back-gate voltage $V_B = 0$ V, $V_{DS} = 1$ V, T_{GOX}=5nm, T_{BOX}=147nm, Na=0.5*10¹⁴ cm⁻², N_{sub}=4*10¹² cm⁻². Curve a: T_{Si} = 8.6 and curve b: T_{Si} =18.2
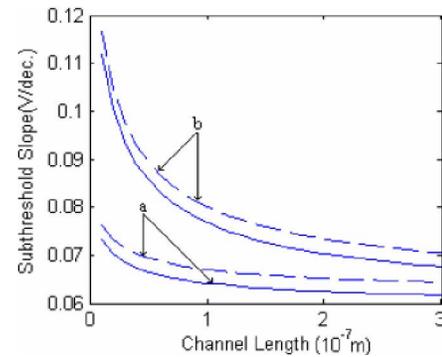

Figure 5 : Plot of Subthreshold slope with channel length for SOI (dashed line) and SON (solid line) MOSFET. Parameter values are same as in figure1 and also the symbols have the same significance
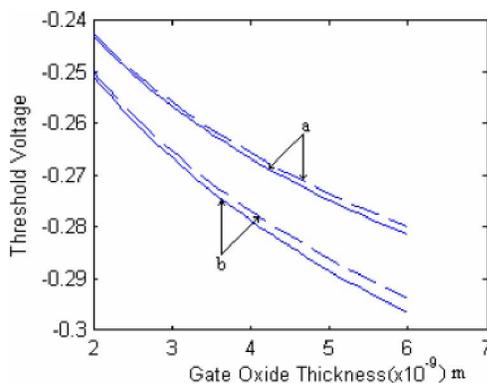

Figure 6 : Threshold voltage with gate oxide thickness for SON (dashed line) and SOI (solid line) MOSFET. Back-gate voltage $V_B = 0$ V, $V_{DS} = 1$ V, T_{BOX}=147nm, Na=0.5*10¹⁴ cm⁻², N_{sub}=4*10¹² cm⁻², L=50nm. Curve a: V_{DS} =1V and curve b: V_{DS} =0.05V. Other parameters are same as in figure 1
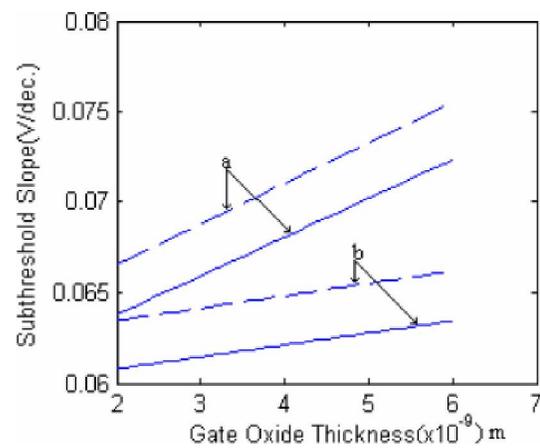

Figure 7 : Subthreshold Slope with gate oxide thickness for SOI (dashed line) and SON (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6

$$C_{Si,d}^{eff} = \frac{dQ_d}{d\Psi} = \frac{qN_A^* t_{Si} L_{eff}}{\Psi_{S1} - \Psi_{S2}} \qquad (3)$$

Here Q_d is the total charge per unit area in silicon in the channel.

DIBL due to fringing field

In isolated channel structure like SOI/SON, penetration of fringing-field lines from source and drain through buried layer or air induces a potential at the channel back interface, which causes fringing field related DIBL. Substrate bias is also capacitively coupled to the channel back interface potential which acts as another source of DIBL. Another DIBL effect is due to accumulation of holes, which are generated by impact ionization, at the channel back interface[17].

Fringing field effect in a fully depleted SOI/SON MOSFET is responsible for a dramatic increase of DIBL[5]. The effect of fringing field can be reduced by using lower dielectric constant material in the BL. This is actually done in SON structure by using air in the BL. Two-dimensional potential profile in the BL is quite complex. As a result, two-dimensional analysis of the fringing field effect has not been developed properly[6]. A compact model of fringing field induced parasitic capacitance can be developed based on conformal mapping technique.

A schematic view of SOI/SON MOSFET with fringing-field lines emanating from the drain to the channel region is shown in figure 3. Assuming that the source is at zero potential, fringing field emanating only from the drain side is considered in the present analysis. Using conformal mapping, the original structure can be converted into an equivalent two-plate system with an angle of inclination of 180 degree as shown in figure 3. The
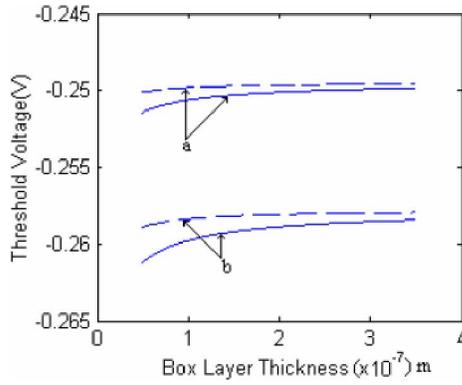
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Figure 8 : Threshold voltage with gate oxide thickness for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6
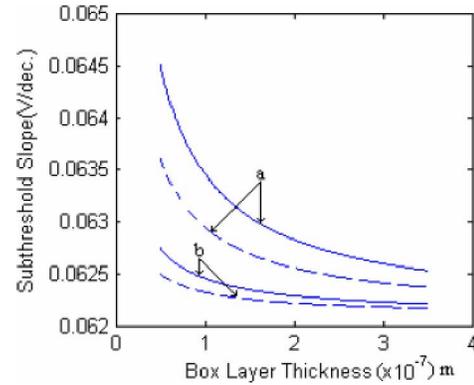

Figure 9 : Subthreshold slope with gate oxide thickness for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6

channel back interface and drain back interface are considered as the two plates which are assumed to be of unit area. The two plates are separated by the depletion layer formed at the channel-drain junction.

The capacitance of the two plates can be calculated using the approach adopted for calculation of capacitance of an inclined plate capacitor with a degree of inclination up to 180 degree[18,19]. The capacitance per unit longitudinal length of the line is[18];

$$C_F^{D/S} = C_F^{in} + C_F^{out} \qquad (4)$$

Here C_F^{in} is the inner capacitance and C_F^{out} is the outer capacitance. For the structure considered here both the capacitances will be same and,

$$C_F^{D/S} = 2\varepsilon_{BL/air} \frac{K^{'}(k_{in/out})}{K(k_{in/out})} \qquad (5)$$

Here, $K'(k_{in/out})=K(k'_{in/out})$ and using the same approach as in Ref. 20 we can write;

$$k_{in/out} = \sqrt{\frac{L_P(L_P + L_F + L_D)}{(L_P + L_F)(L_P + L_D)}} \text{ and}$$

$$k'_{in/out} = \sqrt{\frac{L_F L_D}{(2L_P + L_F)(2L_P + L_D)}} .$$

Since the source and drain are heavily doped n+ regions and the channel is p type, an abrupt junction will be formed with a depletion width of L_P. If device metallurgical channel length is L then effective channel length L_F=L-2*L_P and $L_{D/S}$ is the length of the drain/source side. As $K(k_{in/out})$ is the complete elliptic integral of first kind, taking the expansion, the final expression of the capacitance is expressed as ;

$$C_F^{D/S} = 2\varepsilon_{BL/air} \frac{\left\{ \begin{array}{l} 1 + \left(\dfrac{1}{2}\right)(k'_{in/out})^2 + \left(\dfrac{1.3}{2.4}\right)(k'_{in/out})^4 \\[2mm] + ... + \left(\dfrac{(2n-1)!}{2n!}\right)(k'_{in/out})^{2n} \end{array} \right\}}{\left\{ \begin{array}{l} 1 + \left(\dfrac{1}{2}\right)(k_{in/out})^2 + \left(\dfrac{1.3}{2.4}\right)(k_{in/out})^4 \\[2mm] + ... + \left(\dfrac{(2n-1)!}{2n!}\right)(k_{in/out})^{2n} \end{array} \right\}} \qquad (6)$$

Here, $\varepsilon_{BL/air}$ is the dielectric constant of buried layer/air. As the contribution from the higher order terms is negligible, contribution up to the fourth ordered term is taken into consideration.

Assuming that the substrate is depleted, it can be modeled with an equivalent capacitor C_S which can be calculated from $C_S=\varepsilon_{Si}/W_S$, where W_S is the substrate depletion layer width[11]. The charge induced in the substrate and BL/air interface can be written as $C_S(V_B - V_{FB3})$ where V_B is the substrate bias. For sufficiently thick BL, substrate depletion will be negligible and under such condition C_S can be replaced by a fitting parameter.

Threshold voltage model

Considering equilibrium charge conservation at each node in figure 2, surface potentials ψ_1, ψ_2 and ψ_3 can be expressed as;

$$\psi_1 A + \psi_1 C_{Si,d}^{eff} = C_{GOX}(V_{G1} - V_{FB1}) + C_{Si,d}^{eff}\psi_2 \qquad (7)$$

$$\psi_2 B + \psi_2 C_{Si,d}^{eff} = C_B\psi_3 + (V_{DS} - V_{FB2})C_F^D + C_{Si,d}^{eff}\psi_1 \qquad (8)$$

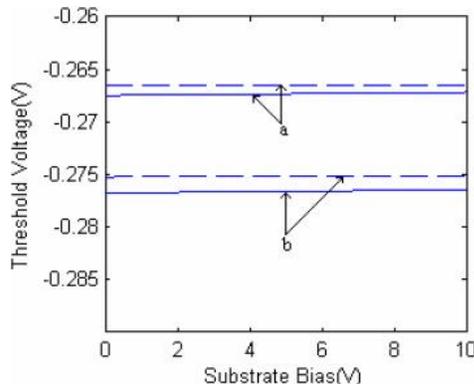$$\psi_3 C = \psi_2 C_B + (V_B - V_{FB3})C_S \qquad (9)$$

Figure 10 : Threshold voltage with substrate bias for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6
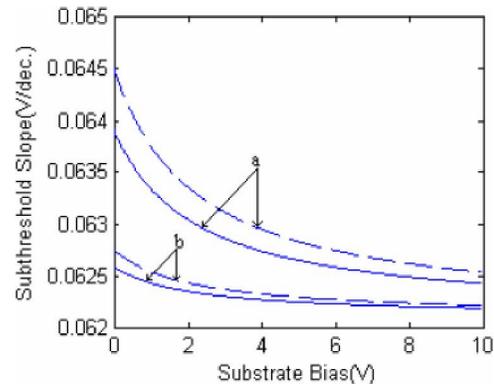

Figure 11 : Subthreshold slope with substrate bias for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6
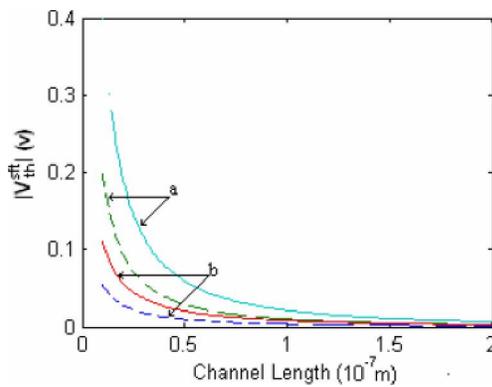

Figure 12 : $\left|V^{sft}_{th}\right|$ with channel length for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6
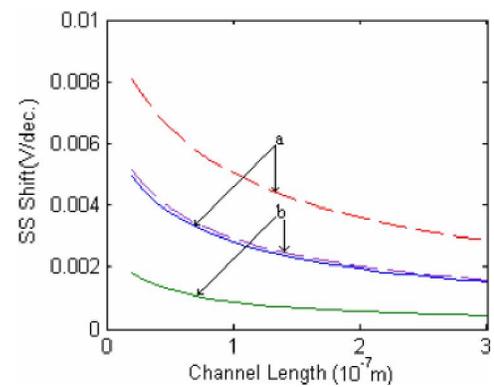

Figure 13 : Subthreshold slope shift with channel length for SON (dashed line) and SOI (solid line) MOSFET. Significance of symbol and parameters values is same as in figure 6

Here, $A=C_{GOX} + C_{if1}$, $B=C_B +C^D_F +C_{if2}$ and $C=C_B + C_S +C_{if3}$. From equations 6, 7, 8 and 9 the following equations are derived;

$$C_3\psi_1 - C_4\psi_2 = C_5 \tag{10}$$

$$-C_6\psi_1 +C_7\psi_2-C_B\psi_3 = C_8 \tag{11}$$

$$-C_B\psi_2 + C\psi_3 = r(V_B-V_{FB3}) \tag{12}$$

Here,

$$C_1 = \sqrt{V_{bi}(V_{bi} + V_{DS})} \ , \qquad C_2 = \frac{2V_{bi} + V_{DS}}{V_{bi}(V_{bi} + V_{DS})} \ ,$$

$$C_3 = A + \frac{2t_{Si}\varepsilon_{Si}}{L_F}(2+C_1C_2) \ , \qquad C_4 = \frac{2t_{Si}\varepsilon_{Si}}{L_F}(2+C_1C_2) \ ,$$

$$C_5 = C_{GOX}(V_{G1} - V_{FB1}) - et_{Si}LN_A + \frac{2t_{Si}\varepsilon_{Si}}{L_F}(V_{DS} + 2V_{bi} + 2C_1) \ ,$$

$$C_6 = 2(2+C_1C_2)\frac{\varepsilon_{Si}t_{Si}}{L_F} \ , \qquad C_7 = B + 2(1+C_1C_2)\frac{t_{Si}\varepsilon_{Si}}{L_F} \ ,$$

$$C_8 = (V_{DS} - V_{FB2})C^D_F + et_{Si}L_FN_A - \frac{2t_{Si}\varepsilon_{Si}}{L_F}(V_{DS} + 2V_{bi} + 2C_1)$$

and r is a fitting parameter, representing resemblance of substrate resistance effect with negligible substrate depletion.

Using Crammer's rule, the expression for $\psi_{1,2}$ and ψ_3 are obtained as;

$$\psi_1 = \frac{CC_5C_7 - C_5C_B^2 + CC_4C_8 + rC_4C_BV_B}{CC_3C_7 - C_3C_B^2 - C_4C_6C} \tag{13}$$

$$\psi_2 = \frac{CC_3C_8 + rC_3C_BV_B + CC_5C_6}{CC_3C_7 - C_3C_B^2 - C_4C_6C} \tag{14}$$

$$\psi_3 = \frac{rC_3C_7V_B + C_BC_3C_8 - rC_4C_6V_B + C_BC_5C_6}{CC_3C_7 - C_3C_B^2 - C_4C_6C} \tag{15}$$

Under the assumption that the inversion layer will be formed at the front interface due to the front interface potential, we can compute device threshold voltage (front channel threshold voltage) by solving V_{G1} in terms of ψ_1 and then replacing ψ_1 with $2\psi_F$. The threshold voltage can be expressed as;

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$$V_{th} = V_{FB1} + 2\psi_F\{(CC_3C_7 - C_3C_B^2 - CC_4C_6) - C_4(CC_8 + rC_BV_B)\}\{C_{GOX}(CC_7 - C_B^2)\}^{-1} \quad (16)$$

In case of bulk MOSFET, threshold voltage is derived from the front interface surface potential ψ_1. The effect of back potential ψ_2 is neglected but in short channel SOI/ SON structure, ψ_1 will be strongly influenced by the back interface ψ_2. Significant modification of ψ_2 in SON structure due to air in the box region will initiate considerable performance variation of SON over SOI structure.

The sub-threshold swing $S = \left(2.3k_BT\dfrac{dV_{G1}}{d\psi_1}\right)$ which can be calculated using eqs.3 and 7 is given as;

$$S = 2.3k_B^T \left\{ \frac{\left(C_{Si,d}^{eff} + \dfrac{A}{C_{GOX}}\right) - C_{Si,d}^{eff}}{\left(B - \dfrac{C_{BOX}^2}{C}\right)} \right\} \quad (17)$$

RESULTS & DISCUSSIONS

Numerical results are simulated using the parameter values given in the TABLE 1.

The plots of threshold voltage and sub-threshold slope with channel length are shown in figure 4 and 5, respectively. The threshold voltage roll-off (TVRO) and subthreshold slope (STS) reduces with increasing channel length due to reduced SCEs with channel length. TVRO predicted by the analytical model is compared with the experimental results of SOI structure available in Ref. 20 and good agreement are obtained indicating the correctness of the model. It is found from both the plots that the TVRO and STS are reduced in case of SON structure compared to SOI structure.

The potential coupling ratio (ψ_1/ψ_2) reduces with decreasing GOX layer thickness. This increases the SCEs thereby increasing the TVRO and STS. The performance of SON structure is found to be superior to SOI structure and their comparison is shown in figure 6 and 7, respectively.

Increasing BL or air layer thickness reduces P_{CR} due to reduced ψ_2 as a result TVRO and STS are reduced. This can be observed in the results presented in figure 8 and 9, respectively.

Variations of threshold voltage and subthreshold slope with the substrate voltage (V_B) are shown in the figure 10 and 11, respectively. Reduction of potential coupling ratio (P_{CR}) with increasing substrate bias explains the nature of these graphs.

Effective shift in TVRO and STS with and without SCEs are plotted with channel length as $|V_{th}^{sft}|$ and S^{sft} in figure 12 and 13, respectively. In case of SON structure, threshold voltage and subthreshold slope shift is minimum due to less SCEs.

CONCLUSION

A three-interface compact capacitive model of horizontal SOI/SON-MOSFET is developed and analytical expressions for threshold voltage and sub-threshold slope have been derived. The SCEs especially DIBL effect due to fringing field, substrate bias and junction-induced lateral field are incorporated in the model. The performance of the two devices are studied and compared in terms of threshold voltage roll-off and sub-threshold slope which are very important issues related to performance analysis of short channel MOSFET. Effect of different parameters like channel length, gate oxide thickness, barrier layer thickness, substrate bias are also investigated and analyzed to understand the comparative performance of SOI and SON structures. Present analysis shows that the SON-MOSFET technology is found to offer devices with scalability and enhanced performance in terms of threshold voltage roll-off and subthreshold slope compared to simple SOI structure thereby providing scope for further miniaturization of devices.

ACKNOWLEDGEMENT

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