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A control method of urban intersection traffic signal based on VHDL

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ABSTRACT

With improvement of the intelligent traffic control systems, the requirements of signal control system are more complex. The traffic signal control circuit are designed and simulated by using hardware description VHDL language in this paper. Considering the traffic flow and intersection signal characteristics, in order to minimize delays in the vehicle at the intersection of control objectives, the implementation of the optimal control signal is introduced in the traffic signal control systems. A method of top-down hierarchical design was used in the system designing, the design of unit circuit was created a module from the bottom to up. Analyses of simulation results using this approach show significant improvement over traditional full-actuated control, especially for the case of accident and over-saturated traffic demand.

KEYWORDS

Traffic engineering; VHDL; Traffic signal systems; Hardware description language; Hierarchical design method.

INTRODUCTION

Signalized intersection is the most basic element in the urban transport network, the studying of optimal control to it is one of the basis points of promoting intelligent transportation systems. Urban transport itself is a random and complex system, and its "real-time" nature in the control process is full of uncertainties. Although the existing traffic control systems agree this point, most of them still use deterministic control method[1 2 3], which can't adjust to the changing factors in reality environment. Reinforcement learning is a new learning method of artificial intelligence, and it has a strong adaptability to the changing environment. Based on the reinforcement learning, this paper proposes a new traffic control model, and the urban traffic signal control circuit is designed by the language of VHDL which is used to descript hardware. This model can friendly adapt to the dynamic traffic environment of the signalized intersection[4 5].

Since 1987 when the VHDL(Very High Integrated Circuit Hardware Description Language) is defined as the standard of IEEE(IEEE-STD-1076), it has become an important tool during the design of digital system and greatly improved the design quality and efficiency. VHDL has the strong ability to describe behaviors and rich simulation statement. Therefore this thesis applies the VHDL language to design the traffic signal control system of multiple intersections and given cycle, which will shorten development time, improve work efficience and reduce the costs, and so on[6].

REINFORCEMENT LEARNING ALGORITHM BASED ON CMAC

In recent years, the reinforcement learning method which takes use of neural network to approximate MDP optimal value function and optimal strategy gets widespread attention and research[7, 8]. The model of neural network of CMAC, which is being used to simulate the function of human cerebellum, has the advantages of partial generalization and fast convergence of learning. Currently, it has been successfully applied to the field of robot control, and it is applied to the field of traffic control in this paper[9].

Q-learning is one of the most commonly used reinforcement learning algorithm, and the SARSA(λ) algorithm is a form of Q-learning based on policy. SARSA comes from quintuple of (s, a, r, st, at) and respectively represents current state, current action, return, next state and next action. The calculating formula of instantaneous differential TD is as follows:

$$\delta = r + \gamma Q(s', a') - Q(s, a) \tag{1}$$

In the formula, Q(s, a) represents current state and action, γ is the discount factor, and the values of Q can be calculated by the approaching of CMAC network. The formula is shown as follow

$$Q(s,a) = f(\phi(s,a), w) = \sum_{i=1}^{N_p} \phi_i(s,a) w_i \tag{2}$$

In the formula, Np is the physical address space dimensions of network of CMAC, $w = (w_1, w_2, \cdots, w_{N_p})$ is the weight vector of output layer, $\phi(s) = (\phi_1(s), \phi_2(s), \cdots, \phi_{N_p}(s))$ is the eigenvector of physical address space. Assuming that C is the generalized parameters, when the state is s, there is a activation unit of C corresponding to an input state in the physical address space, the values of eigenvector is shown as follows:

$$\phi_i(s) = \begin{cases} 1 \\ 0 \quad \text{else} \end{cases}, \text{ (unit of I is activa} \quad i = 1,2,\cdots N_p \tag{3}$$

The exploration and use of action selecion in reinforcement learning is a key problem, the action selection strategy adopts Softmax algorithm, the Softmax algorithm will select the corresponding action based on the probability distribution of Q values:

$$\Pr(a \mid s, Q) = \frac{e^{Q(s,a)/\tau}}{\sum_{b \in A} e^{Q(s,b)/\tau}} \tag{4}$$

In the formula, τ is temperature parameter which is used to control the distribution of Agent exploration. When the temperature is a little higher, all the actions will be selected at equal probability, which is equivalent to the random selection. When the temperature is a little lower, those actions with large Q values will be more likely to be selected. When τ tends to zero, Softmax will convert to greedy algorithm. In this paper, automatic lowering temperature treatment is applied to τ. In the initial stage of Agent learning, in order to guarantee the quick search of Optimal solutions, Agent often adopts exploration actions, so τ will be endowed larger values. With the increasing of Agent learning process, Agent converges, and gradually reducing the temperature until zero. The temperature parameter of i-th learning chatting is shown as follows:

$$\tau_i = \tau_{\min} + \left(\frac{\bar{x}_i - \theta_1}{\theta_2} \right)^2 (\tau_{\max} - \tau_{\min}) \quad \textbf{(5)}$$

In the formula, $\tau_{\max}$ and $\tau_{\min}$ are respectively the maximum temperature and the minimum temperature values; θ_1 and θ_2 are constants; $\bar{x}_i$ is learning chipped before i-1, and it is also the average steps that the Agent takes when it explore the best condition.

$$\bar{x}_i = \frac{1}{i-1} \sum_{j=1}^{i-1} x_j, \quad i = 2,3,\cdots \quad \textbf{(6)}$$

After the algorithm convergence, the lowering temperature treatment avoids the fluctuation which results from the unnecessary exploration action.

SYSTEM FUNCTIONS AND DESIGN REQUIREMENTS

Assuming the intersection is composed by the intersection of main roads and branch roads. The green time of main road is 65 seconds and the branch road is 30 seconds. There are 5 seconds' yellow transition between the green and the red. Under the control of the human, the green time of main roads can keep effective and the red time of branch roads keep the state. When the human control signals are invalid, the state of each signal timing diagram is shown in Figure 1. The high voltage stands for the lights on and the low voltage stands for the lights off[10].

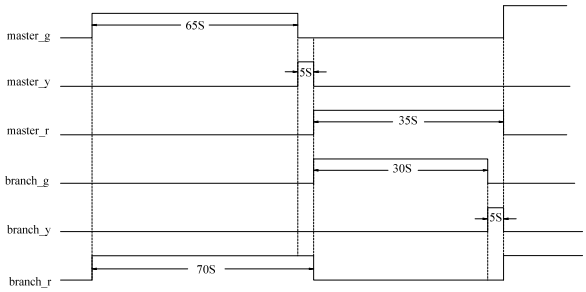

Figure 1 : The timing diagram for given cycle traffic control system

When the state of the main roads or branch roads is green or red, the system can display the remaining time of the allowing or banning in seconds. The system clock can be gotten from the transformation of the power of 50Hz. Assuming we have gained the TTL-compatible square wave signal of 50Hz.

Depending on the design requirements, The system can be divided into four parts. They are pre-divider circuit, master controller, trunk lights down counter, branch lights down counter. Through the pre-divider circuit, 50Hz signal can be divided by 5, 50. The resulting signal of 10Hz can be used to the clock signal of main controller, and the resulting signal of 1Hz can be used to the trigger signal of down counter. Master controller which is the core of the system produces the corresponding signal to control the lights on the main or branch roads. All signals used to control the lights must meet the requirements shown as Figure 1. Meanwhile, the core controller can output the Enable signal to drive the down counter. Under the control of enable signals, trunk lights down counter can complete the 65s' countdown and 35s' countdown, and the output signal can be displayed after decoding. As the trunk lights down counter, Branch lights down counter can complete 70s' countdown(red light on) and 30s' countdown(green light on) under the control of enable signals, and the countdown information can be displayed after decoding. Based on the above analysis, the system block diagram of given cycle traffic signal control system are show on Figure 2.

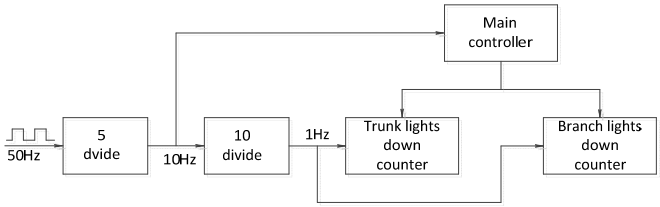

Figure 2 : The block diagram of the system

The design of this system adopts a top-down hierarchical design method. As to the top-level design module, its inputs include 50Hz square wave signal and reset signal. And the outputs include the control signals of red lights, green lights, yellow lights and the 8421BCD signals of countdown counter. The block diagram of top-level design module is shown as Figure 3.

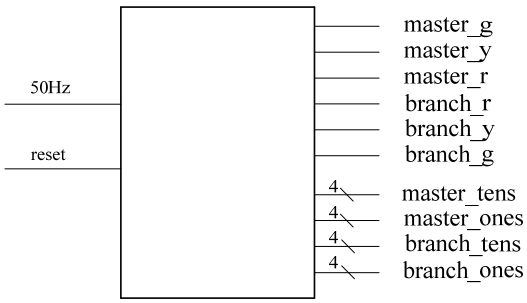

Figure 3 : Block diagram of top-level design module

As to the lower level, it can be divided into four parts to design according to the functions. They are pre-divider unit, main control unit, trunk lights down counter unit and branch lights down counter unit. The block diagram of unit-level in hierarchical design is shown on Figure 4.

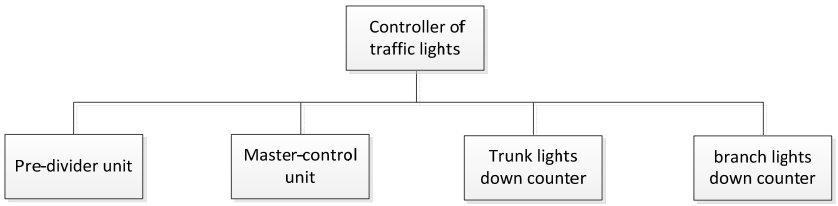

Figure 4 : Block diagram of unit-level in hierarchical design

As to the main control unit, its inputs include 10Hz square wave signal and the reset signal, and its outputs include the control signal of green lights, red lights and yellow lights on main roads or branch roads.

THE DESIGN AND SIMULATION OF MAIN CONTROL MODULE

The input of pre-divider module is 50Hz square wave signal, and its outputs are 10Hz and 1Hz square wave signals. They can be used to the clock pulse signal of main controller or countdown counter separately. Considering the specific requirement of the divider circuit, counting state will be treated as a variable. The definition of port only takes account into the signal of carry output. The 5 divider unit and 10 divider unit can be regarded as a component to handle. The simulation waveforms of pre-divider unit are shown on Figure 5.

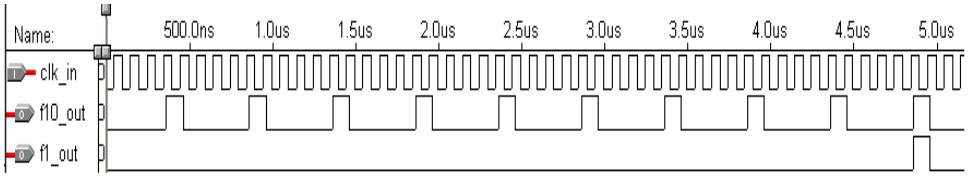

Figure 5 : The simulation waveforms of pre-divider unit

The main functions of master controller are forming the control signals of green lights, red lights and yellow lights under the control of clock signal and reset signal. In order to improve the control accuracy, the cycle time of the input clock waves adopts 0.1s, and the count values correspondingly expand 10 times. There are two processes in this program. One of the two is main-control timing process which is used to realize the finite state machine (four states). The other of the two is auxiliary program which is used to realize the status decoding.

The main controller applies the component of count_k to preset the initial count value when it is in the different states. Then the main controller begins to conduct subtraction counting. It will output a pulse when the initial value equals zero. This pulse will make finite state machine enter next state. The result of the simulation to the main controller is shown on Figure 6. After analyzing, the result can meet the design requirement.

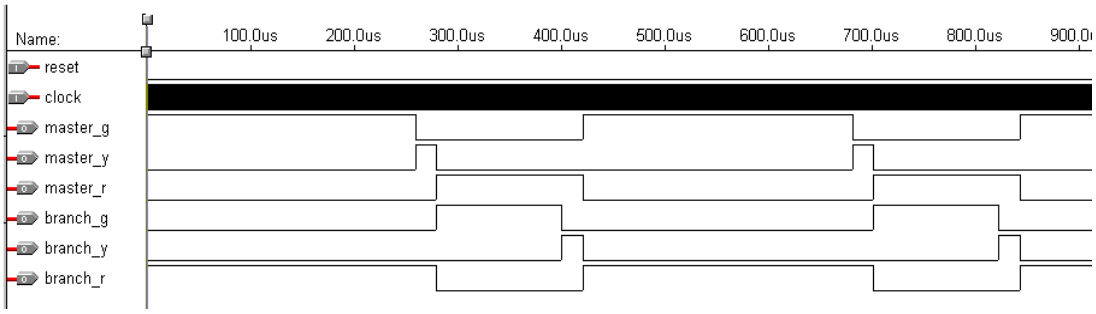

Figure 6 : The simulation of main controller

The input of seven-segment display decoder is the output of every counter, the form of its signal is 8421BCD. And its outputs are the driving signal of the seven-segment digital tube. These signals will be represented by a, b, c, d, e, f. At the same time, assuming the LED is common cathode LED. For programming convenience, we adopt standard logic bit vector (display) to represent, just as display=[a, b, c, d, e, f]. As the non 8421BCD, we require the digital tube keep off. Because of the digital range of tens in second-bit and minute-bit is between 0 and 5. This will consume 3 bits. If it adopts the same seven-segment digital tube with its ones, we must deal with these signals through Concatenation operation. The VHDL files of six-band and ten-band counters can be regarded as COMPONENT to describe. The COMPONENT which stands for VHDL files includes all the important information. In the VHDL files of describing the mold 60 counter, the component is defined at first time. Then name of the component and the key word of PORT MAP will be together to describe the connections among these components.

Simulation result analysis: trunk yellow light on, branch red light on, the counter begins to count down from 5 till zero. At this time, trunk red light on and branch green light on. When the counter counts down from 60 to zero, then the trunk red light keeps on, and the branch have 5 seconds' yellow light time. At this time, trunk green light on and branch red light on, and it will keep 35 seconds. Therefore, this system can meet the requirement of the traffic control system.

CONCLUSIONS

VHDL has the strong ability to describe behaviors and rich simulation statement. Therefore it has been the important tool in the process of the design of digital system. Therefore this thesis applies the VHDL language to design the traffic signal control system of multiple intersections and given cycle, which will shorten development time, improve work efficiency and reduce the costs, and so on. The result of simulation shows that the design program of this system is right and reasonable. Demonstrating the powerful features and superiority of VHDL language.

This paper proposes a new traffic control model based on reinforcement learning, and the VHDL hardware description language is applied to the urban traffic signal control circuit design, and this model can well adjust to the uncertain changes in traffic conditions. In reality, traffic environment exists many uncertain factors(traffic accident, road maintenance, etc), so the control system must have a strong ability to adapt to the environment, and the system this paper have proposed can well solve this problem. Simulation results show that RL controller can effectively accommodate the fluctuations in traffic, and the effect of controlling is obvious. Compared to the traditional induction control, this model can obviously reduce the vehicles' delay at the intersection.

For the control problems of large and complex transportation network, it can be solved by hierarchical control, and the reinforcement learning can conveniently applied to every hierarchical control model, the next step will be to do this in-depth study.

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