Int. J. Chem. Sci.: 14(4), 2016, 3025-3036
ISSN 0972-768X
www.sadgurupublications.com

DESIGN OF HIGH SPEED OPTIMIZED VEDIC MULTIPLICATION TECHNIQUES

D. RAJASEKAR[a*] and E. ANBALAGAN[b]

[a]Pallavaraja College of Engineering, KANCHIPURAM (T.N.) INDIA
[b]Kanchi Pallavan Engineering College, KANCHIPURAM (T.N.) INDIA

ABSTRACT

This paper proposed "The design of ALU using the techniques of Ancient Indian Vedic Calculation" that has been modified into improve performance. The speed of Arithmetic and Logic Unit depends mostly on multiplier. The Vedic Calculation is the ancient system of mathematics which has been a unique techniques of calculation based on 16 Sootra. The work has proved and compared the efficiency of Urdhva-Triyagbhyam vedic method for multiplications which strikes a difference in the actual process of multiplications itself. It generate parallel generation of intermediate products, eliminates unwanted multiplications steps with 0's and scaled to MSB bit levels using Karatsuba algorithm (Divide and Conqure) with the compatibility to different data types. Geometric progression accumulate is an extensible block using in the Vedic multipliers module plays an important role in computing, especially DSP. The coding is done in verilog Hardware Description Language and the Field Program Gated Array syntax is done using Xilinix Spartan library. The result show that Vedic multiplications is efficient in terms of area and velocity compared to conventional multiplication.

Key words: Vedic mathematics, Urdhva triyakbhyam sutra, Karatsuba - Ofman algorithm.

INTRODUCTION

Multiplier have an important effects in designing arithmetic progression, signal and systems, Digital image processors. Many mandatory functions in such processor make use of multipliers "Example, "the basic building blocks in FFTs and MAC" are multipliers". The advanced DSP now have faster bit parallel multiplier embedded.

Various method exist for reduction in computation time involved by the Geometric progression with other factors are trade off. High speed, bit parallel Geometric progression can be classified into Theirs (1) "shift and arithmetic progression that generate partial product sequential and accumulates. This requires much more hardware and it is slowest

*Author for correspondence; E-mail: starsraja@gmail.com

multipliers. This is basic of the array multipliers making to use of the classical multiplying technique which consumes more time to perform twice subtask, addition's and shifting of the bits and hence consumes two to eight cycles of clock period". (2) "Generate all the partial products bit in parallel and accumulates then using a multi operate adder. This is also called a parallel multiplier. By using this technique of Wallaces tree[1] and Booth algorithm"[2], (3) "Using array of most identical cells for generation of bit products and accumulation".

The uses of Vedic calculation show its applications in fast "multiplications, division, squaring, cubing, square roots, cube roots, trigonometry's, three dimensional co-ordinate geometry, solution of plane and spherical triangles, linear and non-linear differential equations, matrix and determinants, log and exponential"[15]. The most interesting point is to note that the calculations provides unique solution in several problems where trial and error method's is available at present.

Vedic calculation offers a fresh and highly efficient approach to mathematics covering a wide range's of starts with elementary multiplication and concludes with a relatively advanced topic, this solutions of non linear differential equations. But the Vedic scheme is not simply a collection of rapid methods; it is a system, a unified approach.

This paper propose a multiplier providing the answer of the critical problems adopting the sootra of Vedic calculation called Urdhva Tiryakbhyam (straight and Cross wise)[3-5]. It can be shown that the designs is highly efficient in term of silicon area/speed.

Using this Vedic technique various ALU module can be designed and integrated to a Vedic Arithmetic Logic Unit, which is compatible for Coprocessor.

Vedic mathematics

Vedic calculation is the part of four Vedaas (books of wisdoms). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an sup vedaas of Atharva Veda. It gives explanations of several mathematical terms including arithmetic (AP), geometry (GP), plane, co-ordinate, trigonometry, quadratic equation, factorizations and even calculus.

His Holiness Jagathguru Shankarachariya Bharathi Krishnan Terthaji Maharaja (1884-1960) comprised all this work together and introduce its mathematical explanations which discussing for various applications. Shankarachaiya constructed 16 sootras (formulae) and 16 sub formulae after elaborate research in Atharva Veda. This formulas are not to be found in present text of atharva veda because these formulae were constructed by himself.

Vedic calculations is not only a mathematical wonder it also a logical. That's why it has degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic mathematical has already crossed the boundaries of India and also become an interesting topic of researching in abroad. Vedic mathematic deals with number of basic as well as complex mathematical operations. Especially, methods of basic arithmetic(AP) are extremely simple and powerful[3,2].

The word "Vedic is derived from the word "Veda which means the store-house of all knowledge. Vedic calculation is mostly based on 16 Sootras dealing with various branches of mathematics like arithmetic, algebra, geometry, log, exponential etc. These Sootras along with their brief meanings are enlisted below.

1. Anurupyee Shunyaamanyat – If 1's in ratio, the other is 0's.
2. Chalana Kalanabyhame –Similarities and Differences.
3. Ekadhikina Purveena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchiyah – The factors of the addition is equal to the addition of the factors.
6. Gunitasamuchiyah – The multiplication of the addition is equal to the addition of the multiplication.
7. Nikhilam Navatashicaramam Dashiatah – All from NINE and last from TEN.
8. Paraavartiya Yojayeti –Adjust and Transpose.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana viyavakalanabhyam – By subtraction and by addition.
11. Shesaniyankena Charamina – The remainder by the last digit.
12. Shuniyam Saamiyasamuccaye – When the addition is the same that addition is zero.
13. Sopaantiyadvayamantyam – twice the penultimate and ultimate.
14. Urdihva-tiryagbhiyam – crosswise and Vertically.
15. Vyashtisamanstihe – Whole and Part Whole.
16. Yaavaduniam – Whatever the extentds of its deficiency.

These methods and ideas can be directly applied to plain and spherical geometry, trigonometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sootras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sootras were also discovered at the same time, which are not discussed here. The beauty of Vedic calculation lies in the fact is reduces the cumbersome looking calculation in conventional mathematics to a very simple one. Because the Vedic formulaes is claimed to be based on the natural principles on which the human mind works. This is a very interesting field and effective algorithms can be applied to various branches of engineering such as computing and DSP[1,4].

The architecture can be classified into three categories. (1)"First is the serial multiplier which emphasizes on hardware and minimum amount of chip area". (2)"Second is the parallel multiplier (tree and array) which carries out very high speed mathematical operations but the drawback is the relatively larger chip space consumptions". (3)"Third is parallel-serial multiplier which serves a good trade off between the time consuming serial multipliers and the space consuming parallel multiplier.

Design of proposed alu module

Urdava – Triyagbhiyam (Crosswisw and Vertically)

Urdava tiryakbhiyam Sootra is a general multiplications formula applicable to all cases of multiplications. It slight means "crosswise and Vertically". To spread this multiplication scheme, let us consider the multiplication of two decimal numbers (2314 × 5498). The conventional method already know to as will require 15 addition and 16 multiplication.

An alternative method of multiplication using Urdava tiryakbhuyam Sootra is shown in Figure.1. The numbers to be multiplied and written on two consecutive side of the squares as shown in figure. The square is divided into columns and rows where each column/row corresponds to one of the digits of either a multipliers or a multiplicands. Thus, each digits of the multipliers as a small box common to a digits of the multiplicands. These small box are partitioned into two halves by the crosswise line. Each digits of the multipliers are independently multiplied with every digits of the multiplicand and the two digits product is written a common box. All the digits lying on a crosswise dotted line were added to the previous carry's. The LSB of the obtained number acts as the result digits and the rest of the carry for next step. Carry for the first step (i.e.) the dotted line on the extreme right side) is taken to be zero.

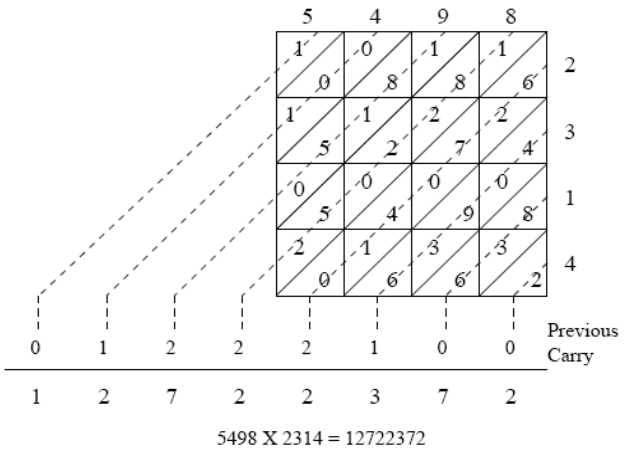

Fig. 1: Alternative way of multiplication by Urdhva tiryakbhyam Sutra

The design starts first with Multipliers designs, that is 2 by 2 bits multipliers as shown in Fig. 2. Here, "Urdava Tiryakbhiyam Sootra" or "Crosswise and Vertically Algorithm"[4] for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is different from the traditional method of multiplication, that is to additional and shifting the partial products.

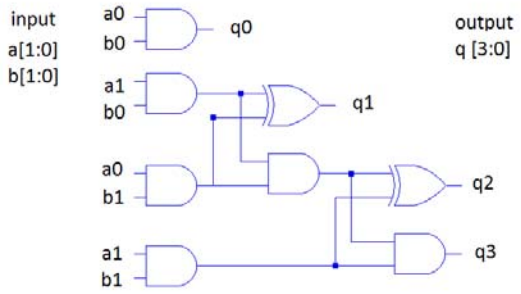

Fig. 2: Hardware realization of 2 x 2 block

To scale the multiplier further, Divide and Conqure algorithm can be employed[6]. Divide and Conqure algorithm is considered as fastest ways to multiply long integers. It is based on the divide and conquer strategy[11]. A multiplication of 2n digits integers is reduced into two n digit multiplication, one (n+1) digit multiplications, two n digit subtraction, two left shift operations, two n digit additions and two 2n digit additions.

The algorithm can be explained as follows:

Let Y and X are the binary representation of two integers:

$$X = \sum_{i=0}^{k-1} x_i 2^i$$

$$Y = \sum_{i=0}^{k-1} y_i 2^i$$

We wish to computing the product YX. Using the divide and conqure strategy, the operand Y and X can be decomposed into equal size parts XL and XH, YL and YH, where subscripts L and H represents high and low order bits of Y and X respectively.

Let k = 2n. If k is odd, it can be right padded with a 0's

$$X = 2^n \sum_{i=0}^{n-1} x_{i+n} 2^i + \sum_{i=0}^{n-1} x_i 2^i = X_H 2^n + X_L$$

$$Y = 2^n \sum_{i=0}^{n-1} y_{i+n} 2^i + \sum_{i=0}^{n-1} y_i 2^i = Y_H 2^n + Y_L$$

The products YX can be computed as follows:

$$\begin{aligned} P &= X * Y \\ &= (X_H 2^n + X_L)(Y_H 2^n + Y_L) \\ &= 2^{2n}(X_H * Y_H) + 2^n((X_H * Y_L) + (X_L * Y_H)) + (X_L * Y_L) \end{aligned}$$

For Multiplier, first the basic blocks, that are the 2 x 2 bit multiplier has been made and then using this blocks 4 x 4 block has been made and then using this 4 x 4 block 8 x 8 bit block 16 x 16 bit block and then finally 32 x 32 bit Multiplier as shown in Fig. 3 has been made[7].

MAC

This unit is built with Vedic multipliers. Hence the advantages of Vedic multipliers like increase in speed, decrease in delay, decrease in power consumption, decrease in area occupied will enhance the MAC unit also. The DSP applications like Convolution (summation of multiplied terms), Correlation, DFT, FFT etc employ the MAC unit, which assists in efficient computing in terms of speed, delay and complexity.

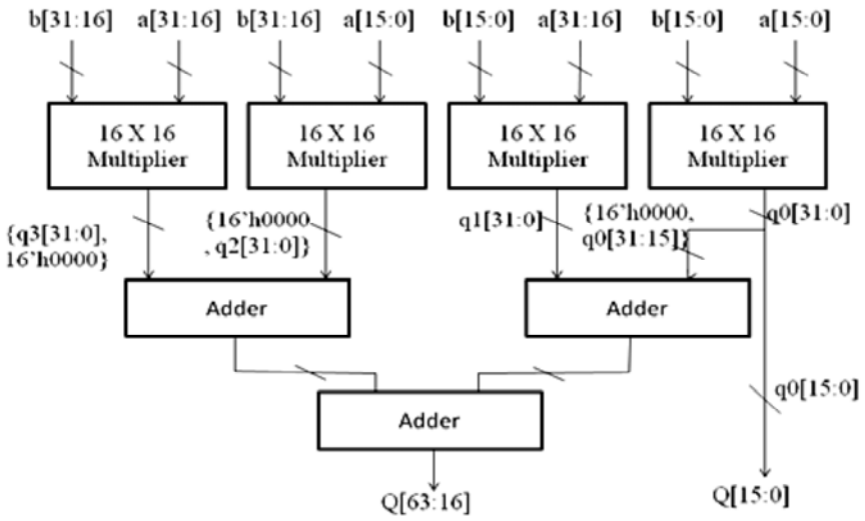

Fig. 3: Block diagram of 32 x 32 multiply block

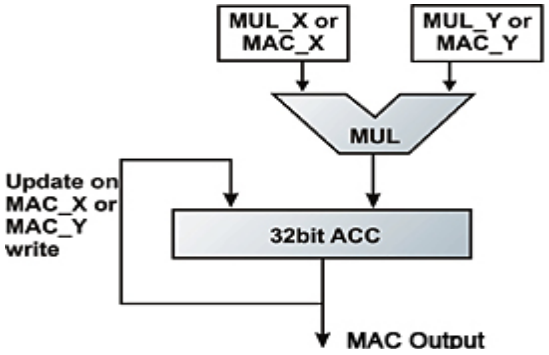

Fig. 4: Multiply and accumulate unit

Design of Adder/Subtractor

Good logic synthesis tools automatically map the "+" operator and "–" onto an appropriate subtractor and adder to meet timing constraints while minimizing the area. For example, the Synopsys Design ware libraries contain carry-ripple adders, carry select adders, carry look ahead adders and a variety of prefix adders.

Design of logic unit

Logic unit consists of AND, OR, NAND, NOR, XOR, XNOR, and INVERTER gates. The inputs of a Logic Unit are A and B with 32-bits, a select line is used for selecting the logic. The output of this is a 32-bit out. The logic unit is show in below Fig. 5.

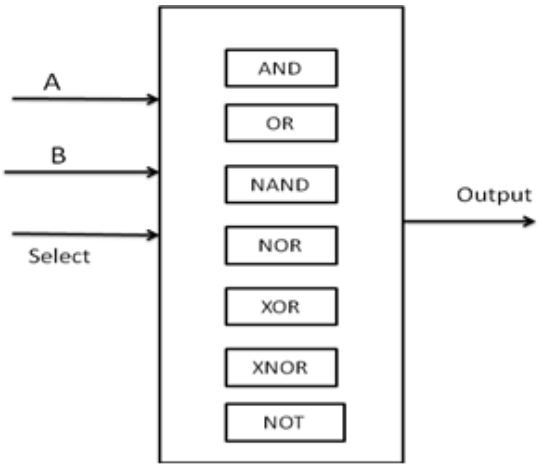

Fig. 5: Logic unit

Arithmetic logic module

ALU can be considered to be the heart of a CPU, as it handles all the mathematical and logical calculations that are needed to be carried out. In this work, an arithmetic unit has been made using Vedic Mathematics algorithms and performs Multiplication, Logic unit, MAC operation as well as addition and subtraction.

For performing addition and subtraction, conventional adder and subtracted have been used. The select signals which tell the arithmetic module, when to perform which operations are provided by the ALU unit.

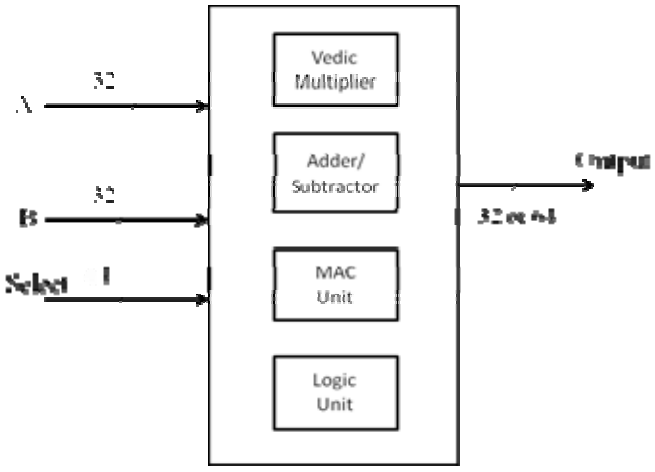

Fig. 6: Arithmetic logic unit

Performance evaluation and comparison

The proposed multiplications were implement using two different coding techniques (1) Conventional shift (2) Add and Vedic technique for 4-8-16-32 bit multiplier. It is evident that there is a considerable increase in speed of the Vedic architecture. The simulation results for 8-16-32 bit multiplier wear shown in the Figs. 7(a) (b) (c), respectively.

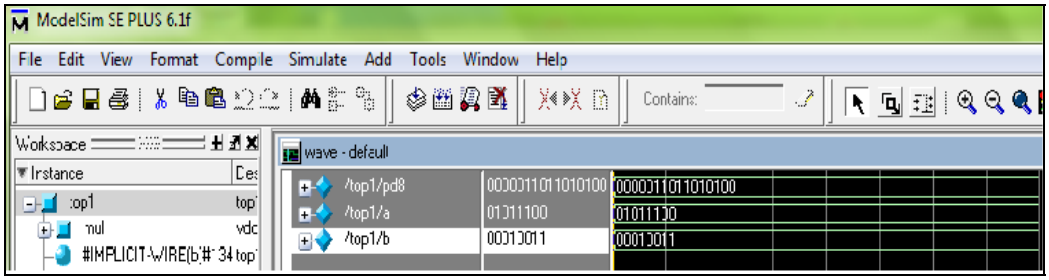

Fig. 7(a): 8 Bit Vedic Multiplier

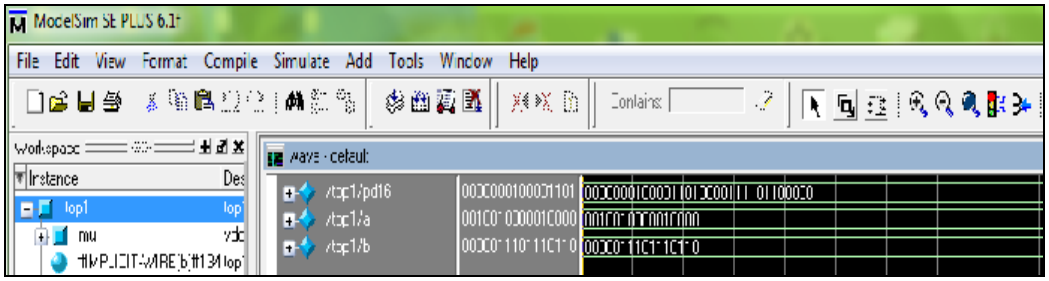

Fig. 7(b): 16 Bit Vedic Multiplier

Fig. 7(c): 32 Bit Vedic Multiplier

The worst cases of propagation delay in the Optimized Vedic calculations case was found to be 31.526ns. To compare it with other implementations the design was synthesize

on XILINIX: SPARTAN: xc3s500e-5fg320[18]. Table 1 show the synthax results for various implementations. The result obtained from proposed Vedic multipliers is faster than Karatsuba Algorithm and Vedic Karatsuba Algorithm.

Table 1: Delay comparison for different multipliers

Size	Algorithm	Delay in ns
8 Bit	Karatsuba Algorithm	31.029
	Vedic Karatsuba Algorithm	18.695
	Optimized vedic multiplier	**15.418**
16 Bit	Karatsuba Algorithm	46.811
	Vedic Karatsuba Algorithm	27.81
	Optimized vedic multiplier	**22.604**
32 Bit	Karatsuba Algorithm	82.834
	Vedic Karatsuba Algorithm	49.864
	Optimized vedic multiplier	**31.526**

CONCLUSION

In this paper, a new method of 32-bit multiplication is presented. The design is based on Vedic calculation of multiplication[9]. This gives has method for higher level multiplier designs. So the designs complexity get reduced for input of large number of bits and modularity get increased. Using this multipliers module the Vedic MAC unit was constructed and both these modules were integrated into an ALU along with the basic adder subtractor and logic unit. The Arithmetic Logic Unit designed with Vedic overlay high speed multiplier algorithm exhibits improved efficiency in terms of speed and area.

REFERENCES

1. C. S. Wallace, A Suggestion for a Fast Multiplier, IEEE Trans. Elec. Comput., EC, **13(1)**, 14-17 (1964).
2. A. D. Booth, A Signed Binary Multiplication Technique, Quarterly J. Mech. Appl. Math., **4(2)**, 236-240 (1951).
3. Jagadguru Swami Sri Bharath and Krsna Tirathji, Vedic Mathematics or Sixteen Simple Sutras From The Vedas, Motilal Banarsidas, Varanasi (India) (1986).

4. A. P. Nicholas, K. R Williams and J. Pickles, Application of Urdhava Sutra, Spiritual Study Group, Roorkee (India) (1984).

5. Neil H. E. Weste, David Harris and Ayan Anerjee, CMOS VLSI Design, A Circuits and Systems Perspective, Third Ed., Published by Person Education, 327-328.

6. M. Ramalatha and D. Sridharan, VLSI Based High Speed Karatsuba Multiplier for Cryptographic Applications Using Vedic Mathematics, IJSCI (2007).

7. H. Thapliyal and M. B. Srinivas, High Speed Efficient N x N Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics, Transactions on Engineering, Computing and Technology, **2** (2004).

8. Jagadguru Swami Sri Bharati Krsna Tirthji Maharaja, Vedic Mathematics, Motilal Banarsidas, Varanasi, India (1986).

9. H. S. Dhilon and A. Mitra, A Reduced-Bit Multiplication Algorithm for Digital Arithmetic, Int. J. Computational Math. Sci., Waset, Spring (2008).

10. Anthony O'Brien and Richard Conway, Lifting Scheme Discrete Wavelet Transform Using Vertical and Crosswise Multipliers, ISSC, Galway, June 18-19 (2008).

11. D. Zuras, On Squaring and Multiplying Large Integers, In Proceedings of International Symposium on Computer Arithmetic, IEEE Computer Society Press, 260-271 (1993).

12. S. Kulkarni, Discrete Fourier Transform (DFT) by using Vedic Mathematics, Papers on Implementation of DSP Algorithms/VLSI Structures using Vedic Mathematics (2006), www.edaindia.com, IC Design portal.

13. S. G. Dani, Vedic Maths': Facts and Myths, One India One People, **4(6)**, 20-21 (2001) (available on www.math.tifr.res.in/ dani).

14. M. C. Hanumantharaju, H. Jayalaxmi, R. K. Renuka and M. Ravishankar, A High Speed Block Convolution Using Ancient Indian Vedic Mathematics, ICCIMA, International Conference on Computational Intelligence and Multimedia Applications, **2**, 169-173 (2007).

15. H. Thapliyal, Vedic Mathematics for Faster Mental Calculations and High Speed VLSI Arithmetic, Invited talk at IEEE Computer Society Student Chapter, University of South Florida, Tampa, FL, Nov 14 (2008).

16. Jeganathan Sriskandarajah, Secrets of Ancient Maths: Vedic Mathematics, J. Indic Studies Foundation, California, 15 and 16.

17. S. Kumaravel and Ramalatha Marimuthu, VLSI Implementation of High Performance RSA Algorithm Using Vedic Mathematics, ICCIMA, International Conference on Computational Intelligence and Multimedia Applications (ICCIMA 2007), **4**, 126-128 (2007).

18. www.xilinx.com

Accepted : 31.10.2016