July 2008 Volume 4 Issue 4

Trade Science Inc.

Materials Science

An Indian Journal

Full Paper

MSAIJ, 4(4), 2008 [321-327]

# Modeling nanoscale MOS capacitors

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*Received: 12th June, 2008 ; Accepted: 17th June, 2008*

## ABSTRACT

The capacitance/voltage characteristics of MOS capacitors with semiconductor and oxide layers of nanometer thickness are modeled by means of equations incorporating the semiconductor and oxide thickness, the doping level and the effects of energy states at the oxide/semiconductor interface and at the semiconductor backside viz the side opposite to the oxide-semiconductor contact. The effect of the semiconductor thickness on the impedance characteristics of the device is introduced by means of a different than zero backside potential. Model equations are derived for both equilibrium and non-equilibrium conditions, practically corresponding to measuring frequencies ranging from below 10Hz up to above 1kHz.



## KEYWORDS

Nanoscale;
MOS;
Capacitor;
Backside potential;
C/V characteristics.

## INTRODUCTION

The development of ultra thin layers of nanometer scale by atomic layer deposition techniques[1], self assembled thin films[2] etc in connection to technological applications requiring ultra thin devices like logic and memory devices, solar cells[3], gas sensors[4], voltage controlled filters[5] and high performance mixed signal applications[6] have promoted the interest for ultra thin MOS structures.

However, for the MOS structures and the Semiconductor-Oxide-Electrolyte (SOE) arrangements[7,8] considered up to now, the nano-scale dimensions refer only to the oxide layer and not to the semiconductor base. The semiconductor substrate is generally assumed to be of practically infinite thickness, which implies that the bulk electrical potential of the semiconductor is equal to zero.

As shown in previous publications[9,10] in MOS structures with semiconductor thickness equal to or less than about ten times the corresponding Debye length this condition is no longer valid. The electrical potential varies from a value $\Psi_S$ at the semiconductor surface to a value $\Psi_{bs} \neq 0$ at the backside of the semiconductor viz the side of the semiconductor layer opposite to the Oxide/Semiconductor interface.

This "back side" potential is an important quantity for the present strategy of modeling MOS capacitors, as long as the effect of the semiconductor thickness on the impedance characteristics of the device is readily introduced by means of $\Psi_{bs}$.

The backside potential can be determined by the numerical solution of Poisson equation for each one of the four operation modes of MOS capacitors, namely the accumulation, flat band, depletion and inversion mode, by the derivation of polynomial expressions relating the surface and the backside potential of the semiconductor in connection to the doping level, the

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oxide and the semiconductor thickness.

Model equations are derived for both equilibrium an non-equilibrium conditions corresponding to measuring frequencies ranging from below 10Hz up to above 1kHz and incorporate the effect of energy states at the Oxide/Semiconductor interface and and at the Semiconductor backside, but not the presence of charges within the oxide layer and the occurrence of work function differences between the Metal and the Semiconductor.

## The electrical potential at the back side of the thin based mos structure

The operation of the MOS structure under equilibrium and non equilibrium conditions is determined by the frequency of the measuring signal. Under low frequencies ( ≥10Hz) majority carriers having very short ($\approx 10^{-12}$s) equilibration times as well as minority carriers with much longer equilibration times ($10^{-3}$-$10^{-4}$s) can follow the variation of the measurement signal. On the contrary under higher frequencies ($\approx 10^{2}$Hz) minority carriers can hardly follow the variation of the measurement signal and at much higher frequencies ($>10^{3}$Hz) become practically immobile, thus not allowing for the formation of inversion layer.

Under low measuring frequencies, the electric field $E_s^{LF}$, at the oxide-semiconductor interface i.e at the surface of a p-type semiconductor, derived by once integrating Poisson's equation is expressed by the relation:

$$E_S^{LF} = \frac{F^{LF}(\psi_s)}{\beta L} \quad (1)$$

where $F^{LF}(\psi_s) = \{2[\cosh\beta\psi_s - 1 + \gamma(\beta\psi_s - \sinh\beta\psi_s)]\}^{1/2}$ (2)

is the so called reduced electric field[9] and $\beta = e_o/kT$, $e_o = 1.6\cdot10^{-19}$C, $\gamma = M/(M^2+4n_i^2)^{1/2}$, M the doping level, $n_i$ the intrinsic carrier concentration and L the effective Debye length given by the known relation:

$$L = \sqrt{\frac{\varepsilon_{si}\varepsilon_o kT}{e_o^2(M^2 + 4n_i^2)^{1/2}}} \quad (3)$$

Under high measuring frequencies the electric field $E_s^{LF}$, of the same MOS structure is expressed by a relation analogous to (1):

$$E_S^{LF} = \frac{F^{LF}(\psi_s)}{\beta L} \quad (4)$$

where the corresponding expression for the reduced field at high frequencies[10] is:

$$F^{HF}(\psi_s) = [(\gamma+1)(\beta\psi_s + e^{-\beta\psi_s}) - \gamma]^{1/2} \quad (5)$$

When a semiconductor layer with finite thickness is considered, then at the backside of the semiconductor there exists a non zero backside electric field, $E_{bs}$ and a corresponding electric potential $\Psi_{bs}$ giving rise to a reduced back side field $F(\Psi_{bs})$ which for simplicity will be denoted as $F_{bs}$.

For a p-type substrate $\Psi_S$ and $\Psi_{bs}$ must always have the same sign except of the case of high negative gate voltages, which is evidently out of the operating conditions of the device. This is also true for $F_{bs}$ and $F(\Psi_S)$.

Therefore, in accordance to the practical operating conditions of the MOS capacitor the following expression which incorporates both $F(\Psi_S)$ and $F_{bs}$ is valid for the reduced electric field $F(\Psi)$:

$$F(\psi) = [F_{bs}^2 + F^2(\psi_s)]^{1/2} \quad (6)$$

Then the Poisson equation set in integral form:

$$\int_{\psi_{G<0}}^{\psi_{G>0}} \frac{d\psi_s}{[F_{bs}^2 + F^2(\psi_s)]^{1/2}} = \int_0^d \frac{dx}{L} \quad (7)$$

may be solved to yield an expression between $\Psi_S$, $\Psi_{bs}$ and the semiconductor thickness d.

Under low frequencies the integral equation (7) takes the form :

$$\int_{accumulation}^{inversion} \frac{dX}{\{F_{bs}^2 + 2[\cosh X - 1 + \gamma(X - \sinh X)]\}^{1/2}} = \int_0^d \frac{dx}{L} \quad (8)$$

where we have set $X=\beta\Psi_S$.

Under high frequencies equation (7) is written as:

$$\int_{accumulation}^{inversion} \frac{dX}{\{F_{bs}^2 + [(\gamma+1)(X + e^{-x}) - \gamma]\}^{1/2}} = \int_0^d \frac{dx}{L} \quad (9)$$

As long as the analytical solution of (8) and (9) is impractical, an approximate solution can be obtained by dividing the overall potential range into parts corresponding to the four modes of operation of the MOS capacitor.

In this way simplified forms of integrals (8) and (9) are derived which can be worked out analytically.

By this approach we can find the relation between the reduced surface potential X and the backside po-

tential $F_{bs}$ which corresponds to a semiconductor thickness d.

When equilibrium conditions are assumed, the expression at the denominator of the left hand side of equation (8) can be written as:

$$\{F_{bs}^2 + 2[\cosh X - 1 + \gamma(X - \sinh X)]\}^{1/2} = \{F_{bs}^2 + 2[e^{-x} - 1 + X + \delta(\sinh X - X)]\}^{1/2} \quad (10)$$

where $\delta = \frac{2n_i^2}{M^2}$

Therefore, within the flat band potential region, where -1=X=1, expression (10) may be simplified according to the following expression:

$$\{F_{bs}^2 + 2[e^{-X} - 1 + X + \delta(\sinh X - X)]\}^{1/2} = (F_{bs}^2 + X^2)^{1/2} \quad (11)$$

At positive values of the surface potential, 1=X=10, the MOS structure operates under the depletion mode. Under these conditions expression (10) may be simplified as follows:

$$\{F_{bs}^2 + 2[e^{-X} - 1 + X + \delta(\sinh X - X)]\}^{1/2} = (F_{bs}^2 + 2X^2)^{1/2} \quad (12)$$

At surface potential values corresponding to the inversion mode (X>10) expression (10) is written as:

$$\{F_{bs}^2 + 2[e^{-X} - 1 + X + \delta(\sinh X - X)]\}^{1/2} = [F_{bs}^2 + 2(X - 1 + \frac{\delta}{2}e^X)]^{1/2} \quad (13)$$

This relation enables to distinguish between to possibilities.

For 0<X<30, $\delta e^x/2 \approx 1$. So expression (13) becomes similar to (12). This is the case of soft inversion.

On the other hand for X>30, $\delta e^x/2 >> X-1$ and expression (13) is written as:

$$\{F_{bs}^2 + 2[e^{-X} - 1 + X + \delta(\sinh X - X)]\}^{1/2} = [(F_{bs}^2 + \delta e^X)]^{1/2} \quad (14)$$

This is the case of strong inversion.

At negative surface potential values, X<-1, the p-type based MOS structure operates under the accumulation mode. In this case expression (10) takes the form:

$$\{F_{bs}^2 + 2[e^{-X} - 1 + X + \delta(\sinh X - X)]\}^{1/2} = [(F_{bs}^2 + 2e^X)]^{1/2} \quad (15)$$

The solution of Poisson equation (8) on account of equations (10) to (15) results to polynomial expressions of $F_{bs}$ as a function of X, under equilibrium conditions, which are illustrated in figure 1 for various doping levels and thicknesses of the semiconductor substrate.

When non equilibrium conditions are assumed the

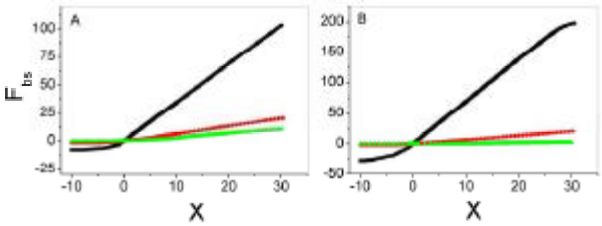


**Figure 1: Reduced backside field, $F_{bs,}$ against reduced surface potential, X, under equilibrium conditions. (A) Doping level M=1.5·10$^{16}$, oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$, ■ 10nm, ● 50nm, ▲ 100nm. (B) Oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$=50nm, doping level ■ 1.5×10$^{14}$, ● 1.5×10$^{16}$, ▲ 1.5×10$^{18}$**

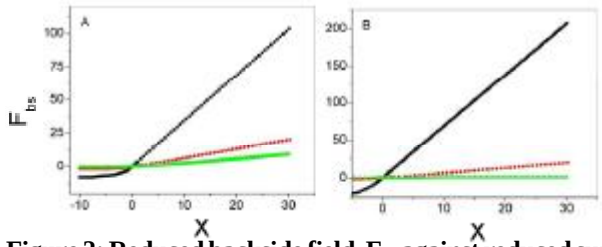


**Figure 2: Reduced backside field, $F_{bs,}$ against reduced surface potential, X, under non-equilibrium conditions. (A) Doping level M=1.5·10$^{16}$, oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$, ■ 10nm, ● 50nm, ▲ 100nm. (B) Oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$=50nm, doping level ■ 1.5·10$^{14}$, ● 1.5·10$^{16}$, ▲ 1.5·10$^{18}$**

expression at the denominator of the left hand side of equation (9) can be simplified to give:

$$\{F_{bs}^2 + [(\gamma + 1)(X + e^{-X}) - \gamma]\}^{1/2} = [F_{bs}^2 + 2(X + e^{-X}) - 1]^{1/2} \quad (16)$$

At surface potentials corresponding to the flat band mode, -1=X=1, expression (16) may be reduced to:

$$[F_{bs}^2 + 2(X + e^{-X}) - 1]^{1/2} = (F_{bs}^2 + 1 + X^2)^{1/2} \quad (17)$$

At positive surface potentials, X>1, we obtain the following expression for both the depletion and inversion modes of operation:

$$[F_{bs}^2 + 2(X + e^{-X}) - 1]^{1/2} = (F_{bs}^2 + 2X - 1)^{1/2} \quad (18)$$

At potentials corresponding to the accumulation mode the denominator of equation (9) is the same for both the equilibrium and non equilibrium conditions, as long as at negative surface potentials the operation of a p-type based device is expected to be the same for either low or high measuring frequencies.

In the case of non equilibrium conditions the solution of Poisson equation (9) on account of equations (15) to (18) results to polynomial expressions of $F_{bs}$ vs X, which are illustrated in figure 2 for various doping

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levels and thicknesses of the semiconductor substrate.

## Model equations for the differential space charge capacitance of thin based mos structures in the presence of energy states within the semiconductor layer

In previous publications[9,10] it was shown that the differential space charge capacitance of a Metal-Oxide-Semiconductor structure with a finite thickness semiconductor substrate under equilibrium and non equilibrium conditions is given respectively by the relations:

$$C_{sc}^{LF} = \frac{\varepsilon_s \varepsilon_o}{L} \cdot \frac{[F_{bs} \frac{dF_{bs}}{dX} + \sinh X + \gamma(1-\cosh X)]}{\{F_{bs}^2 + 2[\cosh X - 1\gamma(X - \sinh X)]\}^{1/2}} \quad (19)$$

and

$$C_{sc}^{HF} = \frac{\varepsilon_s \varepsilon_o}{L} \cdot \frac{F_{bs} \frac{dF_{bs}}{dX} + \frac{1}{2}(\gamma+1)(1-\cosh X)]}{[F_{bs}^2 + (\gamma+1)(X + e^{-X}) - \gamma]^{1/2}} \quad (20)$$

The derivation of equations (19) and (20) is based on the assumption that the electric displacement is continuous through all the interfaces of the metal-oxide-semiconductor arrangement. Therefore, this assumption does not account for the existence of a work function difference, $\Phi^{M/S}$, between the metal and the semiconductor and the subsequent presence of charge, Q, within the oxide layer.

Nevertheless, the reliability of our results is not reduced as long as the condition $\Phi^{M/S} \neq 0$, which implies the presence of such a fixed charge Q at the oxide-semiconductor interface, modifies the flat band condition simply by displacing the C/V characteristics along the voltage axis by a constant amount equal to $Q/C_{ox}$, where $C_{ox}$ is the oxide layer capacitance.

From the so called non ideal conditions we account only for the presence of energy states at both the oxide-semiconductor (O/S) interface and at the semiconductor backside-vacuum contact (S/V), which significantly affect the form of the C/V characteristics. The O/S states are rapid states, exchanging charge with the conduction or the valence band both at low and high frequencies. Such states when, for example, they are in poor electrical contact with the oxide layer, may have equilibration times shorter than $10^{-3}$s. The S/V states are slow states so they can exchange charge only under equilibrium conditions.

Both the O/S and the S/V states are single charge

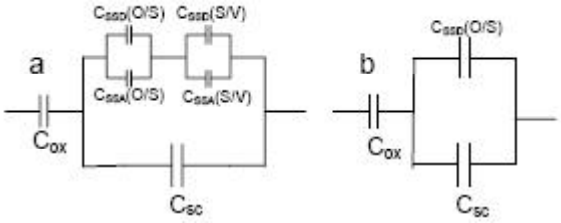


**Figure 3: Equivalent circuits for the MOS structure under low (a) and high (b) frequencies**

surface states of intrinsic origin, with density $N_{SS,}$ which can capture (acceptor like states) or release (donor like states) only one electron, introducing a single allowed energy level $E_{SSA}$ in the forbidden gap close to the conduction band and $E_{SSD}$ close to the valence band.

Under low frequencies both acceptor and donor O/S and S/V states can equilibrate with the measuring signal and be ionized, thus contributing to the surface states differential capacitance.

Under high frequencies the elimination of the contribution of minority carriers also affects the ionization of interface states. In a p-type semiconductor under high frequencies only donor O/S states can be ionized, provided that their characteristic frequency is comparable to that of the measurement signal.

The charge resulting from the ionization of the energy states is given by:

$$Q_{ss} = e_o N_{SS} F_{SS}(X) \quad (21)$$

where: $F_{SSD}(X) = [1+\exp(-\Delta E_{SSD}/kY + X - \sinh^{-1}M/2n_i)]^{-1}$ (22)

and $F_{SSD}(X) = [1+\exp(-\Delta E_{SSD}/kY - X + \sinh^{-1}M/2n_i)]^{-1}$ (23)

are the distribution functions of donor and acceptor states according to Fermi-Dirac statistics.

In (21),$N_{ss}$ is the density of interface states($N_{ss}$ for the donor states and $N_{ssa}$ for the acceptor states) and $\Delta E_{SSD}$ and $\Delta E_{SSA}$ is the difference between the energy of the donor states $E_{SSD}$ and acceptor states $E_{SSA}$ respectively from the value of the intrinsic energy level, $E_i$, at the surface[11].

Therefore, the corresponding expressions for the differential capacitance due to the donor and acceptor states are respectively the following:

$$C_{SSD} = e\beta N_{SSD} \frac{dF_{SSD}(X)}{dX} \quad (24)$$

$$C_{SSA} = e\beta N_{SSA} \frac{dF_{SSA}(X)}{dX} \quad (25)$$

The capacitance components of the MOS structure under examination in equilibrium and non equilib-

rium conditions are combined in the equivalent circuits shown in figures 3a and 3b respectively. The equivalent circuits were defined according to the following points:

**(a)** The total charge within the semiconductor film is:

$$Q_S = Q_{SC} + Q_{SS} \quad (26)$$

**(b)** As long as there is no distance and no particular potential drop, different than that of the space charge, associated with the total surface states capacitance of both the O/S and S/V states, $C_{SS}$, then we obtain:

$$C_S = \frac{dQs}{dX} = \frac{dQ_{SC}}{dX} + \frac{dQ_{SS}}{dX} = C_{SC} + C_{SS} \quad (27)$$

which implies that the space charge and the surface states capacitances are in parallel combination.

**(c)** However, the O/S and the S/V states are located at different points of the semiconductor film justifying the existence of a geometrical distance and a potential drop between them. Thus they can be considered as connected in series, which entails:

$$\frac{1}{C_{SS}} = \frac{1}{C_{SS}(O/S)} + \frac{1}{C_{SS}(S/V)} \quad (28)$$

**(d)** Within each of the capacitance components $C_{SS}$(O/S) and $C_{SS}$(S/V) the capacitance contributions from the acceptor and donor states are in parallel combination, which implies that:

$$C_{SS}(O/S) = C_{SSA}(O/S) + C_{SSD}(O/S) \quad (29)$$

$$\text{and } C_{SS}(O/V) = C_{SSA}(O/V) + C_{SSD}(O/V) \quad (30)$$

In the case of an ohmic metal contact at the back side of the semiconductor it is suggested[12] that an additional capacitance component, termed substrate capacitance, may be introduced.

However, in our model this contribution is incorporated to the space charge capacitance through the backside charge $Q_{bs}$ which is related to the backside field $E_{bs}$ and the backside potential $F_{bs}$ by the expression:

$$Q_{bs} = \varepsilon_o \varepsilon_s E_{bs} = \frac{\varepsilon_o \varepsilon_s}{\beta L} F_{bs} \quad (31)$$

The equilibrium and non-equilibrium C/V characteristics of a p-type based MOS structure for various doping levels and for the physical simulation parameters shown in TABLE 1 in the absence of energy levels are shown in figures 4 and 5, while the corresponding curves incorporating the effect of energy states at the O/S and S/V boundaries are provided in figures 6 and 7. The thickness of semiconductor layer is set equal to 10-100nm, while a minimum value of 10nm was selected for the oxide thickness in order to ensure that tunneling effects[13,14] are minimized.

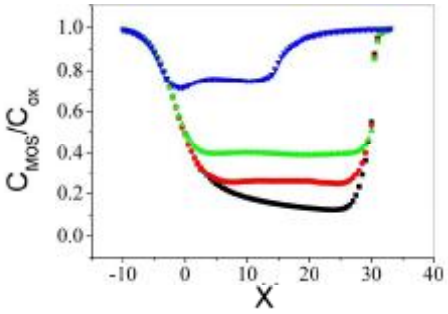


**Figure 4: Equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$: ■ infinite, ● 100nm, ▲ 50nm, ▼ 10nm. Doping level M=1.5E16**

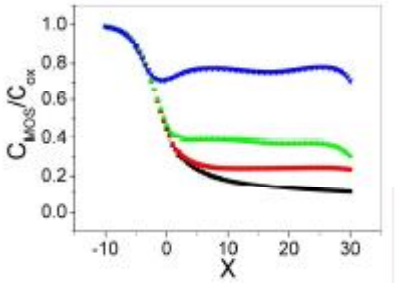


**Figure 5: Non-equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$: ■ infinite, ● 100nm, ▲ 50nm, ▼ 10nm. Doping level M=1.5E16**

**TABLE 1: Physical simulation parameters**

| Parameter | Symbol/Value |
|---|---|
| Permittivity of the oxide layer | $\varepsilon_{ox}$= 3.90 |
| Permittivity of the semiconductor layer | $\varepsilon_S$ = 12.50 |
| Concentration of intrinsic carriers | $n_i = 1.5 \cdot 10^{10} cm^{-3}$ |
| Density of donor surface states | $N_{SSD} = 1 \cdot 10^{12}$ |
| Density of acceptor surface states | $N_{SSA} = 1 \cdot 10^{12}$ |
| Energy difference of onor states at the O/S interface from the intrinsic energy level | $\Delta E_{SSD}(O/S)$= -0.20eV |
| Energy difference of acceptor surface states at the O/S interface from the intrinsic energy level | $\Delta E_{SSA}(O/S)$= 0.25eV |
| Energy difference of donor states at the S/V interface from the intrinsic energy level | $\Delta E_{SSD}(S/V)$= -0.15eV |
| Energy difference of acceptor surface state at the S/V interface from the intrinsic energy level | $\Delta E_{SSA}(S/V)$= 0.35eV |

## DISCUSSION AND CONCLUSIONS

The exploration of the effect of the semiconductor thickness of an MOS structure with both nanometer

scale oxide and semiconductor layer, at a model level, has shown that the thickness effect can be detected over all the thickness range examined from practically infinite ($F_{bs}$=0) to 10nm.

From figures 4 and 5 it is seen that the semiconductor thickness has a profound effect on the C/V characteristics, both at equilibrium and at non-equilibrium conditions. This effect is mainly manifested at thicknesses below 100nm. In this respect, the thin based MOS devices used in practice with thicknesses of the order of $10^{-4}$cm may be assumed to present a typical infinite thickness behavior.

The form of the C/V characteristics, both at equilibrium and at non-equilibrium conditions, is markedly affected by the introduction of energy states at the O/S and S/V boundaries, as illustrated in figures 6 and 7.

Under equilibrium conditions both the acceptor and donor states manifest themselves in the C/V curves in the form of capacitance peaks. States with energy below the intrinsic level ($\Delta E_{SS}$<0) are activated at negative values of the surface potential, while those with energy above the intrinsic level ($\Delta E_{SS}$>0) give capacitance peaks at positive values of X.

Figures 6 and 7 also reveal that the increase of doping level shifts the ionization potential of the boundary energy states, as represented by the peak potential, to more positive values of the surface potential.

At high doping levels exceeding $1.5\cdot10^{16}$ $cm^{-3}$, no capacitance peaks are detected at positive surface potentials, because the capacitance contribution of the energy states is masked by the total capacitance of the MOS structure.

It may be noted that in the systems studied the appearance of capacitance peaks is achieved for energy state densities equal or greater than $10^{11}cm^{-3}$, which is in agreement to literature[15] values.

Under non equilibrium conditions only donor states at the O/S interface can be ionized and so only one capacitance peak emerges.

Other points of interest are the correlation of the thickness of the oxide and the semiconductor film and the contribution of surface states to the total capacitance of the MOS structure.

The variation of oxide thickness affects the C/V characteristics in the absence and the presence of energy states in a more or less predictable way as a consequence of our assumption for the absence of charges within the oxide layer. In particular, the increase of the oxide thickness shifts the C/V characteristics to higher capacitance values over all the potential range, accompanied by a decrease of the extent of variation of $C_{MOS}$/

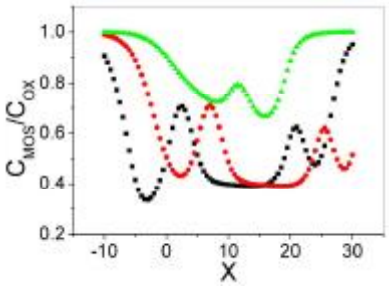


**Figure 6: Equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$=50nm and doping level: ■ $1.5\cdot10^{14}$, ● $1.5\cdot10^{16}$, ▲ $1.5\cdot10^{18}$, in the presence of donor and acceptor energy states at the oxide/semiconductor and semiconductor/vacuum interface as in TABLE 1**

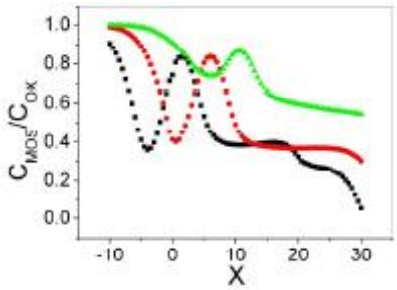


**Figure 7: Non-equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm, semiconductor thickness $d_S$=50nm and doping level: ■ $1.5\cdot10^{14}$, ● $1.5\cdot10^{16}$, ▲ $1.5\cdot10^{18}$, in the presence of donor and acceptor energy states at the oxide/semiconductor and semiconductor/vacuum interface as in TABLE 1**

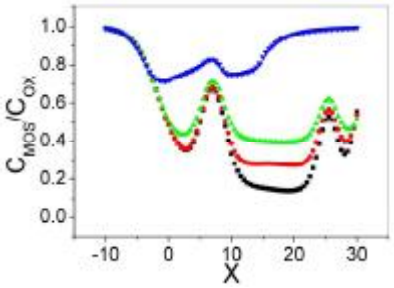


**Figure 8: Equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm and doping level $1.5\cdot10^{16}$. Semiconductor thickness: ■ infinite, ● 100nm, ▲ 50nm, ▼ 10nm, in the presence of donor and acceptor energy states at the oxide/semiconductor and semiconductor/vacuum interface as in TABLE 1**

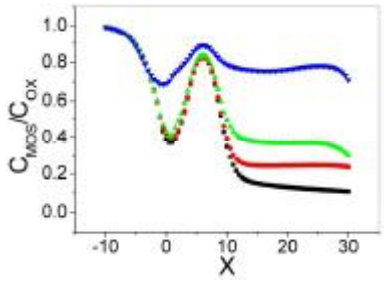


**Figure 9: Non-equilibrium C/V characteristics of MOS capacitor with oxide thickness $d_{ox}$=10nm and doping level $1.5 \cdot 10^{16}$. Semiconductor thickness: ■ infinite, ● 100nm, ▲ 50nm, ▼ 10nm, in the presence of donor and acceptor energy states at the oxide/semiconductor and semiconductor/vacuum interface as in TABLE 1**

$C_{OX}$ values.

On the other hand, the correlation of the semiconductor thickness and the capacitance of the boundary energy states, as shown in figures 8 and 9, reveals some interesting features.

In figures 8 and 9, it is observed that for semicon ductor thickness equal or greater than 50nm the position and height of the capacitance peaks, and thus the ionization of energy states, are necessarily the same with those of the thick base device. On the contrary, the form of the C/V characteristics is markedly changed for $d_s$ values below 50nm, as in the case of $d_s$=10nm.

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