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LOW POWER ASIC IMPLEMENTATION OF LDPC DECODER

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ABSTRACT

In this paper, a low power ASIC implementation of LDPC decoder architecture is presented. The proposed LDPC decoder works based on the principle of min-sum algorithm The proposed LDPC decoder requires limited amount of hard ware resources because of the property of reduced number of iterations in min-sum algorithm because min-sum algorithm is an iteration based error corrector so that we can use the same hardware with limited hardware and the error corrected part is not checked and modified so that we can utilize that hardware for the error correction of other parts or turnoff that so that power can be saved and the iterations required for it also decreases when compared to other decoding algorithms like sum-product and layered decoding algorithms. The other design achieves better Bit Error Rate (BER) performance. After performing synthesis the total area occupied by current design is 1417 (μM^2) and the total power is given as 13.726 (nW). The frequency of current design is obtained as 2.5 MHz. After applying power optimization techniques the total power consumed by current design is reduced by 99.99% when compared to existing design.

Key words: Min-sum, Tanner graph, LDPC, BER, Sum-product, FEC.

INTRODUCTION

In communication system the message bits from the source is given to the transmitter, the transmitter section will modulate the message bits and then given to the encoder. The encoder encodes the data. The encoded data passes through the channel and adds noise to the data and this distorted data is applied to receiver section for decoding the original data. Error detection and correction schemes will helps in detecting errors in the received data and correcting those errors. Extra bits are added to the received data to detect

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the error and the error bits are corrected by using hamming distance method. In Non-binary codes error detection and corrections are done on symbols. In all these methods for higher data error detection and correction requires either larger hardware or time. So to overcome these problems according to current requirements where large amount of data is transferred the alternative method i.e. LDPC. The acronym of LDPC is Linear Density Parity Checker. LDPC decoder is one of the most frequently used forward error correction technique. The decoder used in LDPC is an iterative based min-sum algorithm that performs iterations to decode the original information. LDPC codes are the linear convolution codes widely used in digital video broadcasting standards. Decoding algorithms are classified into two types. In hard decision decoding algorithm threshold voltage detector is used at the receiver end. The detector captures the received signal and checks whether the signal is above threshold level or below, if the received signal is above the threshold level then the output bit is 1 otherwise 0. Next is soft decision decoding algorithm in this additional bits are added as a parity bits for error detection and error correction.

Most of the papers in literature survey consider the LDPC decoder based on sum-product algorithm[1] in serial approach and some other papers considers the layered decoding algorithm[2]. In this paper LDPC decoder works based on min-sum algorithm belongs to the category of soft decision decoder.

Working of LDPC

LDPC code is a linear code with a sparse parity check matrix. Regular LDPC codes are most commonly used in decoder architecture. These codes are represented as (n, wc, wr). Here n is the length of the code word, constant column weight (wc) and constant row weight (wr). The codes are represented in terms of parity check matrix (H). The parity-check matrix H is an (n - k) X n matrix with (n -k) independent rows and n independent columns H is a binary matrix.

$$\text{Parity check matrix } H = \begin{bmatrix} 0 & \cdots & 1 \\ \vdots & \ddots & \vdots \\ 1 & \cdots & 0 \end{bmatrix}_{(n-k)Xn}$$

Tanner graph

LDPC codes are also represented in terms of graphical representation. This type of representation is called as Tanner graph. The graph consists of two types of nodes one is variable node present along the column side and the other is check node present along the row side. The edges in the tanner graph are depends on parity check matrix i.e., in parity

check matrix if first row first column is 1 then the corresponding check node and variable node gets connected.

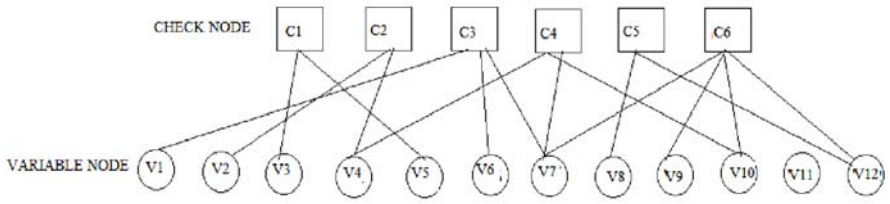

Fig. 1: Tanner graph (graphical representation of parity check matrix)

Proposed LDPC decoder

This section describes min-sum algorithm based LDPC decoder. Min-sum algorithm is the modified version of sum-product algorithm. The performance degradation is reduced by implementing min-sum algorithm. Because min-sum algorithm is an iteration based error corrector so that we can use the same hardware with limited hardware and the error corrected part is not checked and modified so that we can utilize that hardware for the error correction of other parts or turnoff that so that power can be saved and the iterations required for it also decreases.

Working of min-sum algorithm

Min-sum algorithm works in two phases. In first phase check node processing is performed. In second phase bit node processing or variable node processing is performed. Min-sum algorithm works based on the principle of Tanner graph. The operation of min-sum algorithm proceeds as given below: For iteration K, $Y^{K}_{(mn)}$ is the message from bit node n to check node m. $X^{K}_{(mn)}$ is the message from check node m to bit node n. N(m) is the list of adjacent bit nodes for check node m. M(n) is the list of adjacent check nodes for bit node n.

Check node processing: For each m and n belongs to N(m), then

$$X^{K}_{(mn)} = \delta^{K}_{(mn)} Z^{K}_{(mn)} \quad \ldots(1)$$

where

$$Z^{K}_{(mn)} = \min_{n \in N(mn)} \left| Ymn^{K-1} \right| \quad \ldots(2)$$

Bit node processing: For each m and n belongs to M(n), then

$$X^{K}_{(mn)} = X^{0}_{n} + \sum_{m \in M(n)} Xm^{K} \quad \ldots(3)$$

Where $X^0{}_n = Y_n$ …(4)

Flow chart of min-sum algorithm

In receiver section of LDPC decoder consists of three sections. First is initialization, second is bit node processing and third is check node processing. In initialization phase all the previously stored messages at the receiver section is replaced with new messages. In second phase bit node process takes place in this message bits are passed to check node from variable node. In the parity check step check whether received message bits satisfies the condition $CH^T = 0$. This process is also known as syndrome check.

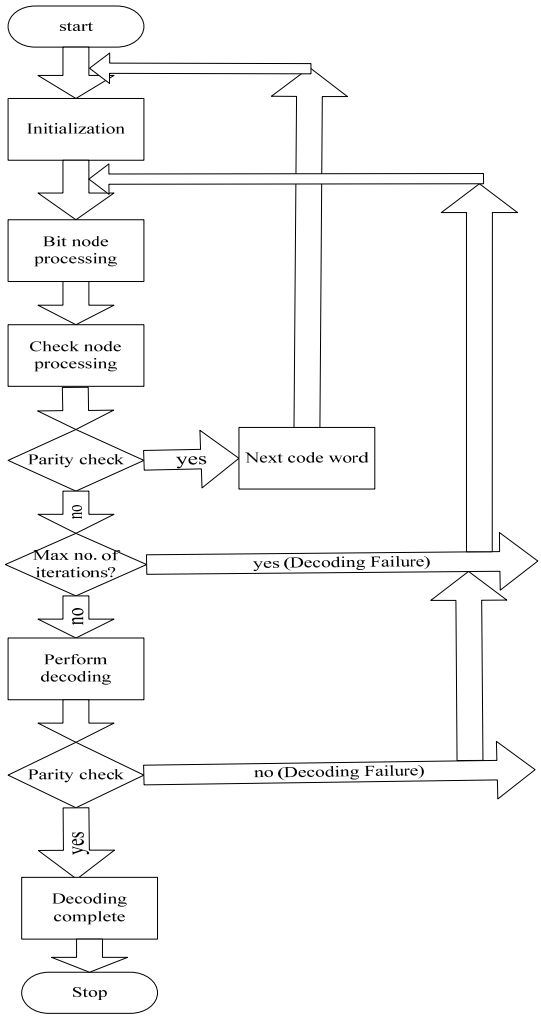

Fig. 2: Flow chart of min-sum algorithm

RESULTS AND DISCUSSION

The proposed min-sum algorithm based LDPC decoder is implemented in ASIC using Synopsys tool in 32 nm technology.

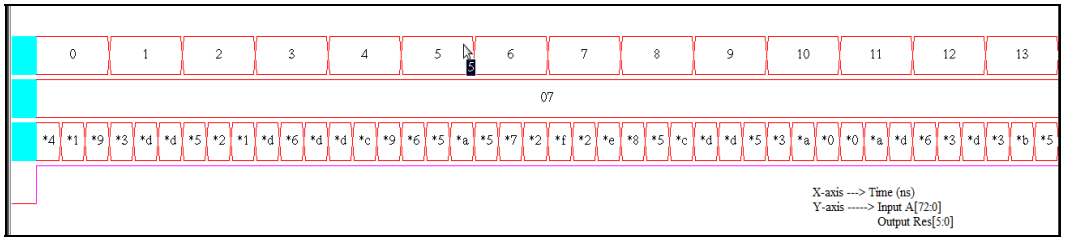

Fig. 3: Wave form of LDPC decoder

The input bit 'A' consists of 72 bit is applied to the receiver side when clock signal is enabled then the decoder output is obtained with 5 bit data. The synthesis is performed to current design to obtain the timing, area and power constraints. The results are tabulated below:

Table 1: synthesis results

Constraints	32 nm Technology
Operating frequency (MHz)	2.5
Total area (μm^2)	5674.5
Total Power (mW)	26.762

The above obtained leakage power is reduced to certain level by applying low power constraints like Multi vdd and Multi vt. In this paper multi threshold low power constraint is applied to reduce leakage power

Table 2: Comparison table

Constraints	Before optimization	After optimization	% reduction in power and area
Total power (nW)	26.762	13.726	99.99
Leakage power (nW)	26.7615	0.000	100
Area (μm^2)	5674	1417	75.02

CONCLUSION

In this paper min-sum algorithm based LDPC decoder is implemented. The results shows that the presented decoder reduces the usage of more number of hardware resources by reducing the incoming message length and also simplifies operation of check node. Therefore interconnect complexity is reduced. The total power consumed by decoder is reduced when compared to sum product algorithm based LDPC decoder because of reducing the number of iterations. The leakage power is further reduced by 99.99% by applying Multi Vt as low power constraints.

REFERENCES

1. J. C. Porcello, Senior Member IEEE, Designing and Implementing Low Density Parity Check (LDPC) Decoders using FPGAs, IEEE Trans. Circuits Syst. II, Exp. Briefs, **62(1)** (2015).
2. Y. Chen, Q. Zhang, D. Wu, C. Zhou and X. Zeng, An Efficient Multirate LDPC-CC Decoder With a Layered Decoding Algorithm for the IEEE 1901 Standard, IEEE Trans, Circuits Syst. II, Exp. Briefs, Dec., **61(12)** (2014).
3. Bertrand Le Gal, Christophe Jego and Jeremie Crenne, A High Throughput Efficient Approach for Decoding LDPC Codes onto GPU Devices, IEEE Embedded SYS, Lett., **6(2)** (2014).
4. Vikram Arkalgud Chandrasetty and Syed Mahfuzul Aziz, An Area Efficient LDPC Decoder using a Reduced Complexity Min-Sum Algorithm, Integration, the VLSI Journal, doi:10.1016/j.vlsi.2011.08.002 45 (2012).

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