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DESIGN OF LINEAR TUNEABLE TRANSCONDUCTANCE (GM) CIRCUIT

VARNINDRA M. SONI and R. SAKHTIVEL*

VLSI Design, School of Electronics (SENSE), VIT University, VELLORE (T.N.) INDIA

ABSTRACT

In this paper, a linearly tuneable transconductor circuit is presented. The transconductance circuit works in sub-threshold region. The transconductance circuit is designed such that it produces linear tuning upto the range of 1us to 8us. The simulation for transconductance circuit is carried out in Cadence Virtuoso tool and the channel length parameter for the design is 45 nm. Since the design operates in subthreshold region, it provides additional advantage of low power**.**

Key words: Transconductor, Subthreshold, Cadence™.

INTRODUCTION

With growing communication market, which demands low power consumption, low cost and gives high performance. While the demand of low power has demerits like poor linearity. We know linearly tunable transconductor are useful building blocks in many analog circuits. The main reason to build transconductance block, which has tunable feature in this design, as it compensates for process variations. This assures that center frequency and quality factor have desired value. To achieve the required programmability, the most common approach is to use MOS transistor in triode region as source degeneration.

The application of tunable transconductor is to select different frequency value by changing value. However, in this work we have tuning range of 8, for compensation of process variation. In Section II, reviews on the previous transconductance designs. In Section III, targets over the design of linearly tuneable transconductance circuit is presented. Our simulation for given circuit and results are laid out in section IV Section V concludes this paper.

*Author for correspondence; E-mail: rsakthivel@vit.ac.in

EXPERIMENTAL

Literature survey

This section portrays CMOS transconductor and its operation in different region and low power design. And moreover it discusses about linearly tuneable aspects of Gm block. Equation (1) does not hold linear relationship with input voltage and output current because of second term.

$$I_{Dl} = K_n (V_{GS} - V_{tn}) V_{DS} - \frac{1}{2} \alpha Kn V_{DS}^2 \quad \ldots(1)$$

Another important factor about transconductance, as device size scales down it does not obey linearity property. So this motivates to consider differential design, since it provides good linearity, high signal to noise ratio.

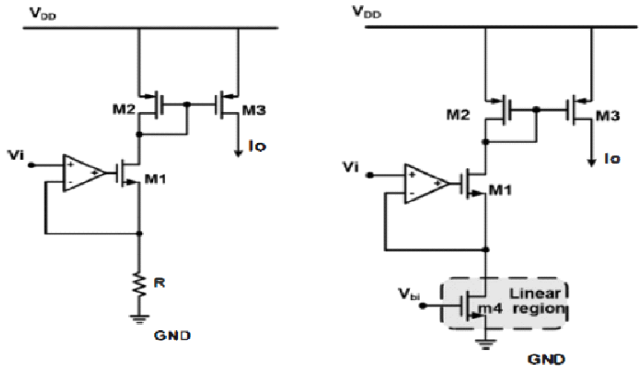

Fig. 1: Transconductor amplifier with (a) Resistor (b) MOSFET

Transconductance amplifier

Our design is targeted to produce good tuneability i.e. for equal change in input voltage produces equal change in Gm value. The design consist of two stage amplifier circuit. The main objective to use this topology, as it provides high gain and good rail to rail voltage.

Voltage to current conversion

In this design, M1-M4 is works in weak inversion or sub-threshold region. The current equation for weak inversion region is shown below equations (2) & (3).

$$V_{GS1} - V_{th} = \eta U_T \, Ln \left(\frac{I_{D1}}{I_{D0}} \times \frac{L_1}{W_1} \right) \quad \ldots(2)$$

$$V_{GS2} - V_{th} = \eta U_T \, Ln \left(\frac{I_{D2}}{I_{D0}} \times \frac{L_2}{W_2} \right) \quad \ldots(3)$$

The transistor sizing M1-M4 are same

$$\Delta V = V_{GS1} - V_{GS2} = V_{GS3} - V_{GS4} = \eta U_T \, Ln \left(\frac{I_1 + i_i}{I_1 - I_I} \right) \quad \ldots(4)$$

For better linearity, M21-M23 transistor are biased such that their region of operation is inear point while tuning the device. The remaining transistors operates in sub-threshold region.

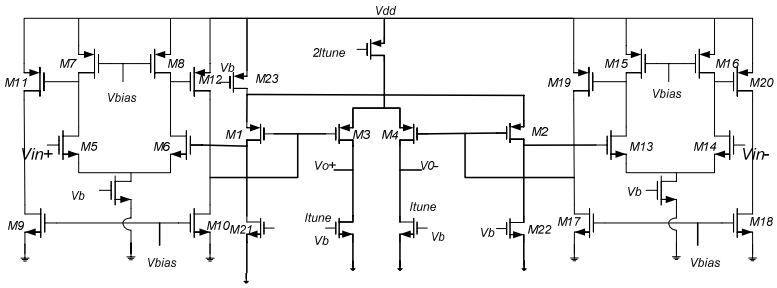

Fig. 2: Transconductance amplifier

CMFB circuit

The Common mode feedback circuit is composed of differential structure, it is to adjust the yield output voltage over whole scope of transconductor. Feedback loop causes output voltage to desired value and it maintains tuneability. Fig. 3 shows Common mode feedback design for tuneability.

Fig. 6 shows simulation results for transconductor with differential voltage input and obtained tuning range is 1us to 8 us. As all transistors work in weak inversion region so Vref is very small to obtain higher Gm.

RESULTS AND DISCUSSION

A linearly tuneable CMOS transconductance is presented. The transconductance topology with CMFB circuit provides a good range tuneable transconductance from 1 μS to 8 μS. The steady state power consumption of the circuit is 1.137 uW.

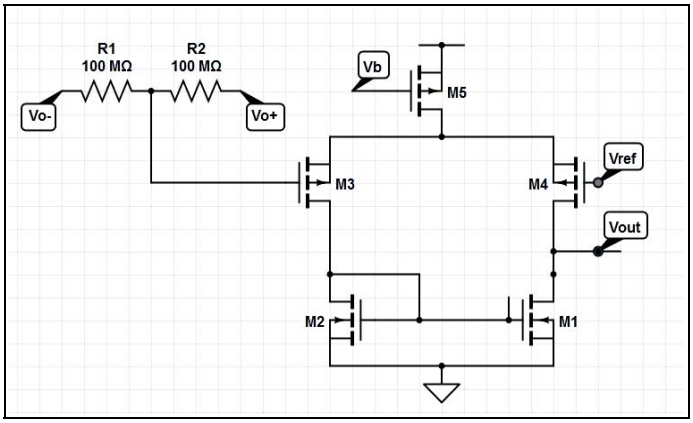

Fig. 3: CMFB circuit

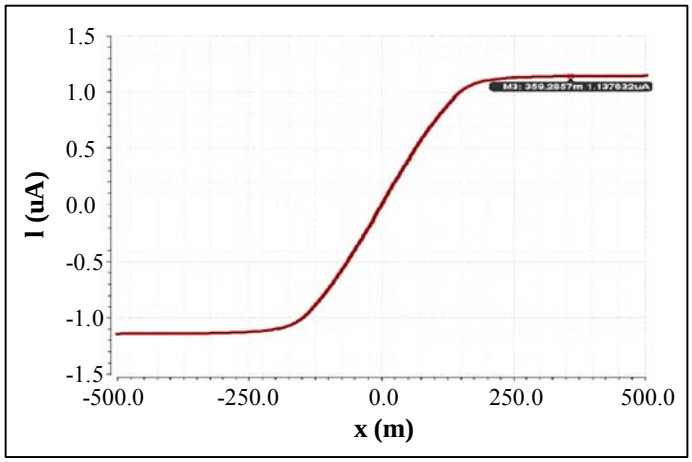

Fig. 4 Output drain current Vs input voltage

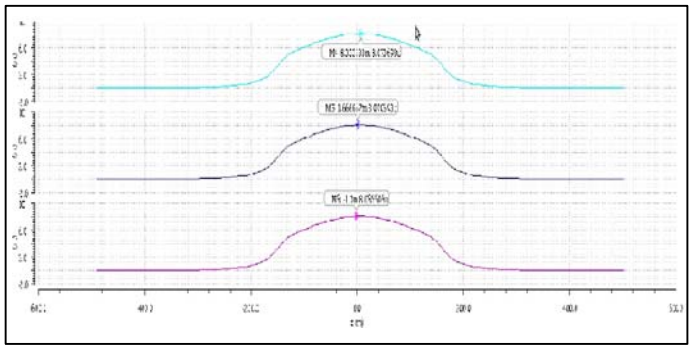

Fig. 5 Output drain current Vs input voltage and transconductance Vs input voltage

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