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A SURVEY: ON VARIOUS PLACERS USED IN VLSI STANDARD CELL PLACEMENT AND MIXED CELL PLACEMENT

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ABSTRACT

The placement technique is to place modules into a fixed outline rectangular die in that, no modules should not overlap with each other and some cost effective parameter (e.g., wire length) is optimized. Placement is an important step in VLSI physical design process. Generally placement algorithms (called placers) can be classified into three major categories: simulated annealing based placers, min-cut based placers, and analytical based placers. According to the recent literature, analytical placers give the best quality in placement in VLSI physical design step. Analytical placers are further classified into two types (i) nonlinear (ii) quadratic. Again quadratic placers are further classified into three types (i) partitioning based quadratic placers (ii) Force directed quadratic placers (iii) Warping based quadratic placers. In this paper, we take a brief survey about the various analytical quadratic force directed placers. This survey paper first introduces the placement problem and then how that placement problem is solved using various techniques in analytical quadratic force directed placement are explained. Finally this paper explains bench marking in various analytical force directed placers in standard cell placement and mixed cell placement and also gives some suggestions for future work.

Key words: VLSI physical design process, Analytical placers, Force directed analytical placers

INTRODUCTION

Placement is the process of identifying the exact locations of modules with in a fixed outline rectangular die surface. It is a very difficult step in VLSI physical design[15] mainly

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for the following four reasons. First, placement plays a key role in circuit performance. Second, placement identifies the routing of that design. Third, placement distributes the heat within that die surface. Fourth, placement decides power consumption of that circuit. So placement problem[16] is an important and interesting problem among many researchers. In physical design[1] before placement floor planning is performed. Floor planning and placement both[15,16] are interrelated to each other. The difference between floor planning and placement is given as, in a fixed rectangular die surface floor planning identifies the relative locations of modules with respect to interconnection requirements whereas, placement identifies the exact locations of modules. In placement sizes and the shapes of all modules are fixed whereas in floor planning sizes and shapes can be changed with respect to fixed aspect ratio. Placement is nothing but a special case of floor planning.

Generally Placement algorithms (placers)[18] are classified into three types (i) simulated annealing, (ii) top down cut based partitioning (iii) analytical. Of these analytical placement[15-18] is a very popular method. This survey paper mainly focuses on analytical placement.

Placement problem

Placement problem is identified as a NP-complete problem[13]. The placement problem is usually divided into the following three sub problems global placement, legalization and detailed placement. In global placement[7,15] the approximate locations of modules and the objective function minimizing wire length (HPWL) is determined. After global placement, HPWL is minimized but overlapping is identified because global placement allows some percentage of overlapping among modules. Overlapping between modules leads to an illegal placement solution. In legalization step, no overlap is allowed; it changes an illegal global placement solution into a legal one. Finally in detailed placement, objective function is further improved by performing local refinements.

Problem formulation

A placement region is a rectangle area[1] defined by coordinates (x_{min}, y_{min}, x_{max}, y_{max}). In recent problems L-shapes or T-shapes have also been used. But, for global placement, a rectangular placement region is still used. The circuit net list is represented as a graph $G = (V, E)$, where V is a set of modules in a design and E is a set of connections (nets) among them. The vertex set V consists of two disjoint subsets, MV and FV where MV/FV represents a set of movable/fixed modules respectively. For each $v \in$ FV, the location (x, y) of v is already determined and the placement should not change them. The location of each

$v \in$ MV needs to be determined by placement and their locations must fall within the given fixed outline rectangular die surface *P*.

Placement objective: Common objective function in placement is minimization of HPWL[7,15,16,18].

$$\text{HPWL}(x,y) = \sum_{e \in E} \left[\sum_{i \in e} \text{maxxi} - \sum_{i \in e} \text{minxi} + \sum_{i \in e} \text{maxyi} - \sum_{i \in e} \text{minyi} \right] \quad \ldots(1)$$

(x,y) in eqn. (1) are the co-ordinates of the blocks inside the rectangular region.

Placement constraints: Common placement constraints are

No overlap: The area occupied by any two modules/cells cannot overlap with each other.

Fixed outline: Each vertex must be placed entirely within a specified rectangular region bounded by $x_{min}(y_{min})$ and $x_{max}(y_{max})$, which denote the left (bottom) and right (top) boundaries of the specified region.

Analytical placement

In analytical placement, placement problem is represented as a mathematical programming, which is also having placement objectives and constraints. The placement objectives are optimized through analytical approaches. Analytical placers can be classified into the following two categories:[15,16] (i) nonlinear placers (ii) quadratic placers.

Examples of nonlinear placers are APlace[2] NTUPlace[3]. High CPU times are needed for these nonlinear placers during optimization. With respect to CPU time, quadratic placers are very popular nowadays. Again quadratic placers are further classified into three types (i) partitioning based quadratic placers like PROUD[4], Gordian[5] (ii) Force directed quadratic placers like FAR[6], Fast place[7], Mfar[8], FDP[14], RQL[10], and Eisenmann's Kraftwerk[18], MAPLE[17], SimPL[16], Polar[15] (iii) Warping based quadratic placers presented in[11,12]. In this survey paper we discus about analytic quadratic force directed placers like[6-8,15-18].

Analytical quadratic global placement

The typical objective of global placement is to minimize its wire length, and a fundamental constraint is to avoid any cell overlap. Global placement is for Wire length estimation and reduction.

Wire length (HPWL) estimation and minimization

The first sub problem in analytical global placement is to estimate and minimize total wire length of a design because minimizing wire length[7,15,16] is a fundamental step to optimize other metrics, such as timing, power and routability of a design. In this paper quadratic wire length minimization can be addressed as the half perimeter wire length (HPWL) based objective function. HPWL is the smallest bounding box, which surrounds all sinks of net. HPWL estimation is defined in eqn (1). HPWL minimization can be performed using quadratic programming in[7,15,16,18].

Quadratic programming for HPWL minimization

The HPWL[7,8,15,16,18] is given by Manhattan distance between the two connected modules .In quadratic placer, the Manhattan distance is approximated by squared Euclidean distance of the two connected modules, so the cost function of global placement can be defined in eqn (2). HPWL can be automatically minimized by minimizing the value of $\Phi\ (\vec{x}, \vec{y})$.

$$\Phi\ (\vec{x}, \vec{y}) = \sum_{i,j} W_{i,j} [(x_i - x_j)^2 + (y_i - y_i)^2] \quad \ldots(2)$$

The objective function that sums up the cost of all the nets can be written in matrix notation as

$$\Phi\ (\vec{x}, \vec{y}) = \frac{1}{2}\ x^T Q_x x + c^T x + \frac{1}{2}\ y^T Q_y y + c^T y + \text{const} \quad \ldots(3)$$

Where Q_x, Q_y are both sparse symmetric positive-definite system of linear equations. The objective function Φ is minimized by solving the linear system in eqn. (4).

$$Q_x x + cx + Q_y y + cy = 0 \quad \ldots(4)$$

eqn(4) can be solved using eqn(5) and eqn(6) [for *x* and *y* directions]

$$Q_x x + cx = 0 \quad \ldots(5)$$

$$Q_y y + cy = 0 \quad \ldots(6)$$

To solve eqn (5). A fast and accurate technique is needed .Since matrix Q_x sparse, symmetric, and positive definite, we solve eqn (5) by the preconditioned conjugate gradient method. The incomplete cholesky factorization of matrix is used as the preconditioner[7,15,16]. According to[7,15,16,18] the solver runtime is directly proportional to the number of nonzero

entries in matrix. In order to have minimal nonzero entries in matrix Q_x *a* good net model is required. Because a good net model contains only two-pin nets for the circuit this in turn, reduces the non zero entries in matrix Q_x.

Net models

A multi pin connection (in real circuit) increases the non zero entries in matrix Q_x. A net model is used to compose every multi pin net in real circuit into set of two pin connections. The net models can be classified as Clique, Star, hybrid (clique + star) and Bound to Bound (B2B). Viswanathan and Chu[7] explained the equivalence of the star net model and the clique net model. Hence, both net models (clique and star) can be used interchangeably. Clique net model is used for small nets (i.e., nets with a low number of pins). The star net model is used for big nets (i.e., nets with a high number of pins).

[Kraftwerk 2][18,15,16] the new bound 2 bound net model is based on the idea of removing all inner two-pin connections and utilizing only connections to the boundary pins. With this, the boundary pins span the net, and the property of the HPWL net length being the distance between the boundary pins is emulated.

Overlap reduction technique

However, minimizing just quadratic wire length would lead to considerable cell overlapping. Therefore, many techniques have been proposed to remove this cell overlapping reduction.

Force directed method

In force-directed approach is used to reduce overlapping. In this method, cells are gradually spread out until the cell distribution is almost even and the wire length is not improved any more. Examples of quadratic placers which apply force-directed approach are Kraft werk 2[18], mFAR[8], Fast Place[7], RQL[10], SimPL[16], POLAR[15] and MAPLE[17].

Spreading forces using fixed point technique

Force directed method is handled in different ways in different placers. Kraftwerk 2[18], it is based on density gradient. Kraftwerk 2[18] utilizes a poisson potential by a generic supply and demand system, while, Fast Place[7] and RQL[10] move the cells from high density bins to the low density bins by cell shifting. Recently, Sim PL[16] proposed a new cell spreading technique called look-ahead legalization. In MAPLE[17], the look-ahead legalization of SimPL [p] is combined with multilevel clustering and improved by iterative local refinement[7].

From the above various techniques, fixed point technique (mFAR)[8] is a famous one which is used in POLAR][15] and SimPL[16] to reduce the cell overlapping.

Table 1: Summarizes the above techniques in various popular analytical force directed placers

Placers	Wire length model	Overlap reduction	Integration	Optimization
Kraftwerk[18]	Bound 2 Bound (B2B)	Density (Poisson)	Fixed point	Quadratic
mFAR[8]	Quadratic	Density (Poisson)	Fixed point	Quadratic
Fastplace[7]	Quadratic (hybrid)	Cell Shifting	Fixed point	Quadratic
RQL[10]	Quadratic (B2B)	Cell Shifting	Fixed point	Quadratic
Maple[7]	Quadratic (B2B)	ProLR (Progressive local refinement)	Fixed point	Quadratic
SimPL[16]	Quadratic (B2B)	LAL (Look ahead legalization)	Fixed point	Quadratic
Polar[15]	Quadratic (B2B)	LAL (Look ahead legalization)	Fixed point	Quadratic

Placement in various placers

Global placement plays an important role in final placement. So, global placement is discussed in detail in the following example placers.

Global placement in various quadratic force directed placers

[kraftwerk 2][18] Initially modules are spread over the chip, If initial overlap is >20% create supply demand system (D) then computes the poisson potential Φ. After Φ calculation B2B model is applied to identify two pin connections then, the system is solved using linear equations and module positions are updated per iteration. [Fast place][7] Global optimization involves minimizing the quadratic objective function then cell shifting is performed to remove overlaps. During second step entire placement region is divided into equal-sized bins. Each bin utilization is determined. During third step, spreading forces are added to prevent

the cells from collapsing back to their original positions during the next global optimization. [RQL][10] Global optimization minimizes the quadratic cost function, it has 3 steps (a) Solving the quadratic program (QP) (b) Spread the modules with density constrains and also determine the spreading forces (c) Adding spreading forces to the subsequent QP. [Sim PL][16] is a flat, force-directed global placer, that solves quadratic program using PCG solver. It maintains a lower-bound and an upper-bound placement and reduces the displacement between the two then, the final solution is derived from the upper-bound placement when the two bounds converge.[MAPLE][17] Relies on SimPL. In global placement it performs the following three operations (i) Clustering (ii) Top level placement iterations (iii) Progressive Local Refinement (ProLR) used in conjunction with unclustering.[POLAR][15] Inspired by SimPL in global placement stage, a good wire length-driven seed placement without considering cell overlapping is generated, then it generates hybrid net model. It is responsible to the initial connection matrices, and linear system is solved by PCG to get the initial placement then, B2B net model updates the connection matrices to further optimize the wire length iteration.

Bench marks ISPD2002, ISPD 2005, ISPD 2006

Benchmark suite used for placement can also be used for floor planning and routing. These benchmarks are directly derived from modern industrial ASIC designs and are being used in the first ISPD (International Symposium on Physical Design) placement contest. The primary goal of benchmark is to provide better opportunity in placement algorithms for future placement researchers.[18] uses ISPD05, 06 and ICCAD 2004 (mixed sized bench mark suite),[7] uses ISPD'02 and IBM- MS,[10,15,17] uses ISPD'05and ISPD'06,[16] uses ISPD'05 for their placers.

CONCLUSION

In this survey paper, module placement problem and various placers have been studied. This paper presents a brief survey on the various quadratic force directed placers used in placement problem. In this survey paper, we concentrate mainly on HPWL minimization as a main objective function there should not be any overlap between the modules as a main constraint. This paper does not include any routing constraints, time delay of circuits etc. Although significant progress has been made in recent analytical placement research, some research gap is also identified in modern circuit designs. Many more challenges and opportunities are in modern circuit designs. The future researchers may trying to solve the following placement related issues like, large macro placement,

routability, timing, power, and/or thermal-driven optimization for the analytical quadratic force directed placement problem.

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